Proceedings of the 2023 International Conference on Machine Learning and Automation
DOI: 10.54254/2755-2721/39/20230596

Optimization of 4-bit absolute value detector based on CMOS and PTL

Ju Han[1], Yingning Jia[2,4] and Yuxin Yang[3]

[1]University of Electronic Science and Technology of China, Chengdu, Sichuan, 610000, China
[2]Southeast University, Nanjing, Jiangsu, 210000, China
[3]University of Science and Technology Beijing, Peking, 100000, China

[4]213201113@seu.edu.cn

Abstract. This article designed and optimized a 4-bit absolute-value detector mostly using Complementary Metal Oxide Semiconductor (CMOS) static logic and transmission gate logic (PTL). In terms of overall architecture, the implementation of logic circuit functions is primarily separated into two modules, including the absolute value detector and the comparator. This paper identified the critical path of the final detector and conducted research and simplification on it to improve the general functionality of the detector which can compare the value of two numbers. To shorten the delay time in the circuit, this paper reduced the number of components on the crucial path. After calculating, the critical path delay is approximately 61.065 and the initial energy consumption for a minimum path delay is 51.06. To obtain the least amount of delay and energy use, three different techniques were used in this investigation. Ultimately, we found that the circuit optimized using the "Changing V_{DD} and Sizing" method was the most efficient. The optimized critical path delay remained around 61.065, and the energy consumption under optimized critical path delay was reduced to 10.845. The final implementation achieved a decrease of 82.2% in energy consumption while maintaining the critical path delay unchanged.

Keywords: Encrypted Communication, Digital Signature, Absolute Value Detector, CMOS, PTL.

1. Introduction

Ensuring the security and privacy of data in modern communication has become a critical task [1]. Encrypted communication, which involves encrypting and decrypting data using cryptographic techniques, is widely employed to protect the confidentiality and integrity of sensitive information. Comparators, specifically four-bit logic comparators in this article [2, 3], play a crucial role in the decoding process of encrypted communication. These electronic circuits compare received encrypted data with encryption keys, enabling the recovery of the original information.

This research paper proposes two designs of 4-bit absolute value detectors, one utilizing static CMOS logic and the other incorporating PTL for optimization [4, 5]. These designs combine different types of logic circuits to achieve efficient absolute value detection functionality. The absolute value detectors are crucial components in the overall circuit topology, which includes a 3-bit comparator. The comparator compares the output of the absolute value detector with a predefined threshold value to

DOI: 10.54254/2755-2721/39/20230596

determine whether the input number is greater or smaller. The importance of secure communication and the role of absolute value detectors in encrypted systems highlight the significance of optimizing these circuits for improved performance. This paper focuses on critical path calculation and optimization techniques to minimize energy. By adjusting the value of VDD and the sizing of transistors, the delay can be increased to 1.5 times the minimum delay.

2. Working principle

In the realm of contemporary communication, ensuring the security and privacy of data has emerged as a pivotal undertaking. Encrypted communication, employing cryptographic techniques, has become a widely utilized approach to safeguard the confidentiality and integrity of sensitive information, allowing only authorized individuals to access and comprehend the content [6]. The process of encrypted communication typically encompasses several steps, including encryption, transmission, decryption, and authentication.

In addition to the requirements of high data rates, low latency, and resistance to interference, the demand for maintaining the confidentiality of communication content has become increasingly crucial in the context of ubiquitous connectivity and the global interconnection of devices. Applications such as smart homes, social media platforms, and online shopping websites bring immense convenience to individuals, but they also pose privacy risks due to inadequate confidentiality measures. Encrypted communication plays a vital role in mitigating these risks, ensuring that personal information remains secure and protected.

For instance, in applications involving facial recognition, the extraction of facial feature points can serve as digital signatures for personal information websites, or encrypted communication between smart home devices [7, 8]. Within the process of signal transmission, absolute value comparators can effectively calculate the bit error rate [9]. During signature verification, comparators serve as tools to validate the authenticity and validity of signatures [10]. To facilitate the processing of digital signals by the numerical comparators, certain preprocessing steps are necessary during signal transmission. These steps may include sampling, filtering, and analog-to-digital conversion (ADC). Figure 1 illustrates the encoding and decoding process of raw data.

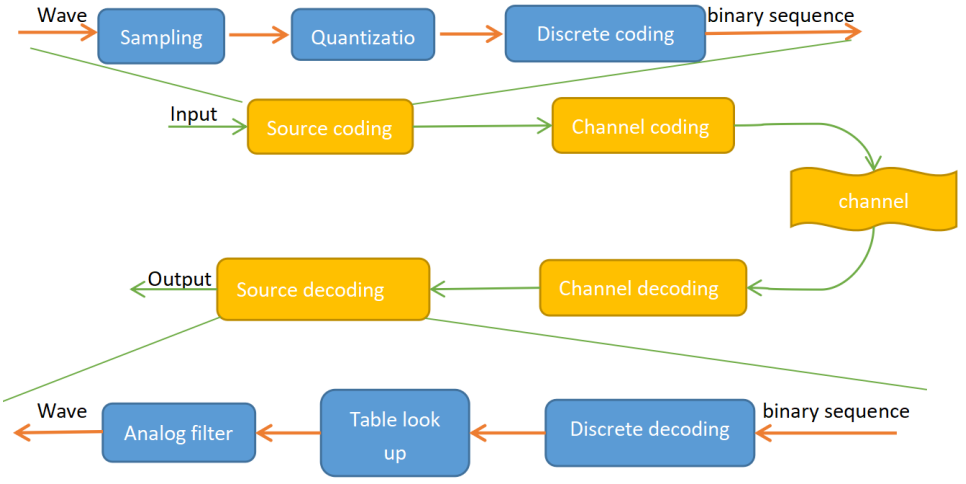

Figure 1. The process of coding and decoding (Photo/Picture credit: Original).

During the process of signal transmission, information undergoes encoding before propagation and decoding at the receiving end. In wireless communication systems, where spectrum resources are non-renewable, ensuring efficient and stable interaction throughout the entire communication system is essential. Source encoding fundamentally involves converting analog signals into binary form. On the other hand, channel encoding serves as the foundation for encrypted communication by replacing original data bits with other bits, thus achieving encryption of the information. The data processed

DOI: 10.54254/2755-2721/39/20230596

through channel encoding is referred to as codewords. To prevent information loss, the length of codewords in the encryption process is often greater than the length before encoding. This means that during the encoding process, additional bits, known as redundancy bits, are added to the original data. Although the inclusion of redundancy bits, which maintain the integrity of the information, reduces deviations caused by noise interference during signal transmission, there is still a possibility that the encrypted algorithm-replaced valid data may not be correctly decrypted. Figure 2 demonstrates the structure of bit error rate (BER) generator. Hence, the introduction of digitally encoded signals after source encoding and decrypted signals after channel decoding as the threshold and operand of the comparator. This approach ensures the correctness and reliability of signal transmission.

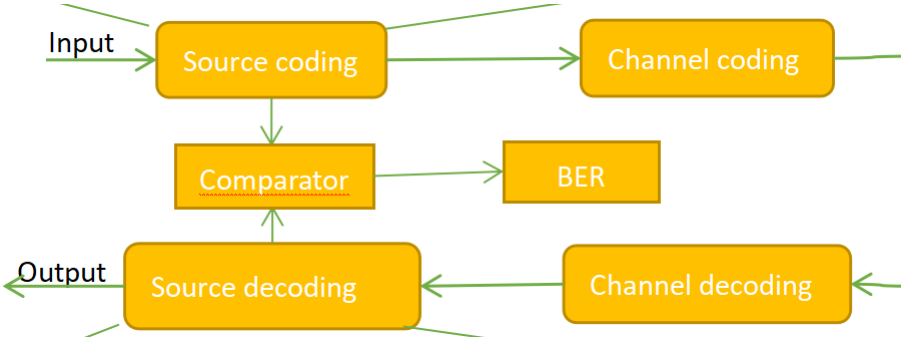

Figure 2. BER detection (Photo/Picture credit: Original).

In addition to being a tool for detecting bit error rates, absolute detectors can perform a similar function in the verification of digital signatures shown in figure 3. Due to the extremely high security of digital signatures: protection against man-in-the-middle attacks and cross-site request forgery (CSRF), it can be well applied to authentication systems: device authentication, user authentication and third-party authentication, etc [11, 12]. Its core working principle is to uniquely prove the identity of the sender by providing identifiable digital information. In such a system, there are usually two complementary types of operations: one is the signing operation and the other is the verification operation. Signing is performed by the sender holding the private key representing the identity, and verification is done by the public key held by the receiver. The determination of identity is achieved by the comparison of hash values, and during the verification process, if the hash value of the data does not match the hash value decrypted by the public key, it can be determined that the operation was not performed by the owner of the private key. The comparison of hash values is achieved using numeric comparators, which are discussed in the following sections.

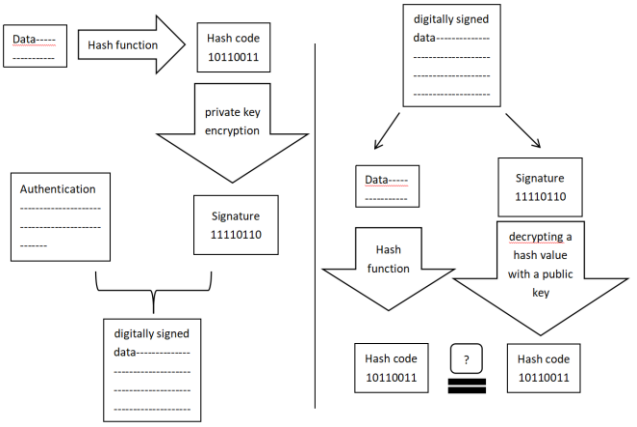

Figure 3. The process of generating digital signature (Photo/Picture credit: Original).

DOI: 10.54254/2755-2721/39/20230596

3. Circuit topology selection

Our final detector is made up of a 4-bit detector which can achieve absolute value conversion and a 3-bit comparator to compare the value of input. The purpose of this part of detector is to determine whether the input number is negative based on the input sign bit. The 3-bit comparator is then given the input's absolute value, which is taken from there. The later comparator compares the number received from the former detector with a given threshold value. The final comparator's output is only "0" or "1". The circuit produces "0" if threshold value is higher than the input value. The circuit outputs "1" when the threshold value is lower than the input value.

3.1. The detector

This detector can achieve absolute value conversion. The sign bit A3 and the contents of the other 3 input signal bits make up the input of this kind of value detector. A3 represents the highest bit of the input, while A0 represents the lowest bit. When the value of A3 is "0", the input is defined as a positive number. When the value of A3 is "1", the input is defined as a negative number. In this case, we need to implement the output as the two's complement of the input when it is negative. Therefore, we can derive the truth table about the value conversion.

Table 1. Truth table for detector values.

A_3	A_2	A_1	A_0	B_2	B_1	B_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	1	0	0
1	1	0	1	0	1	1
1	1	1	0	0	1	0
1	1	1	1	0	0	1

Based on the truth table, we can determine the connection between the inputs and outputs, and subsequently derive the corresponding expression.

$$B_0 = A_3 \oplus \overline{A_0} \tag{1}$$

$$B_1 = \overline{A_1} \oplus (\overline{A_0} \cdot A_3) \tag{2}$$

$$B_2 = ((\overline{A_0} \cdot A_3) \cdot \overline{A_1}) \oplus \overline{A_2} \tag{3}$$

Through the analysis of the expression, we have obtained the final circuit structure for the former detector in figure 4, which consists of inverters, half adders and 2-1 multiplexers.

DOI: 10.54254/2755-2721/39/20230596

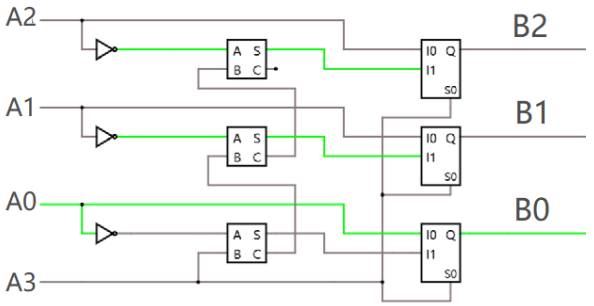

Figure 4. The 4-bit absolute value detector's internals (Photo/Picture credit: Original).

3.2. The comparator

The function of this comparator is to compare the absolute value of the input with a predetermined threshold, in order to determine which value is greater and output the corresponding result. Based on the relationship between the inputs and outputs mentioned earlier, we can directly obtain the truth table for the 3-bit comparator. The 4-bit absolute value detector's outputs (B2, B1, B0) and threshold values (C2, C1, C0) are the comparator's inputs. The output of the comparator will be either "0" or "1" based on the comparison result. The truth table for the later comparator is Table 2.

Table 2. The part of truth table of the later comparator.

B_2	B_1	B_0	C_2	C_1	C_0	Y
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	1	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	0
0	1	1	0	1	0	1
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Based on the truth table, we can observe the output equation (4).

$$Y = (\overline{C_0} \cdot B_0) \cdot (\overline{B_1 \oplus C_1}) \cdot (\overline{B_2 \oplus C_2}) + (\overline{C_1} \cdot B_1) \cdot (\overline{B_2 \oplus C_2}) + (\overline{C_2} \cdot B_2) \quad (4)$$

Through the analysis of the expression, we have obtained the final circuit structure in figure 5.

DOI: 10.54254/2755-2721/39/20230596

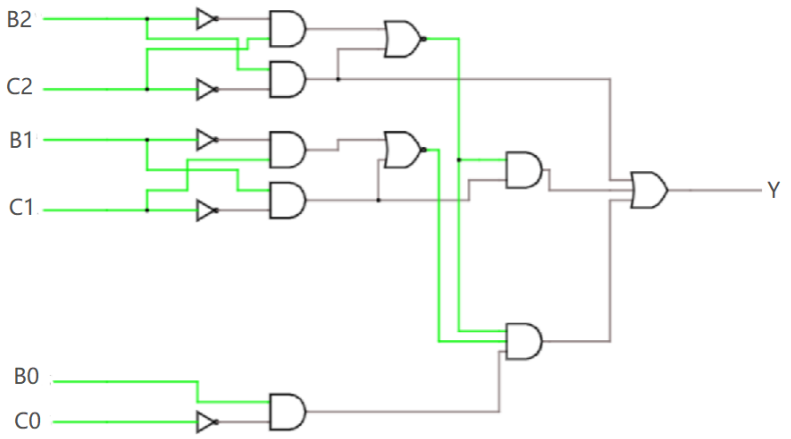

Figure 5. The 3-bit comparator's internals (Photo/Picture credit: Original).

3.3. The final combined structure

By combining the former detector and later comparator in series, the circuit can compare the absolute values of two 4-bit inputs and determine their relationship (greater than, less than, or equal). This allows for the comparison of positive and negative numbers without considering their signs, which means we achieve an absolute-value detector. So it can get the final combined internal of absolute-value detector in figure 6.

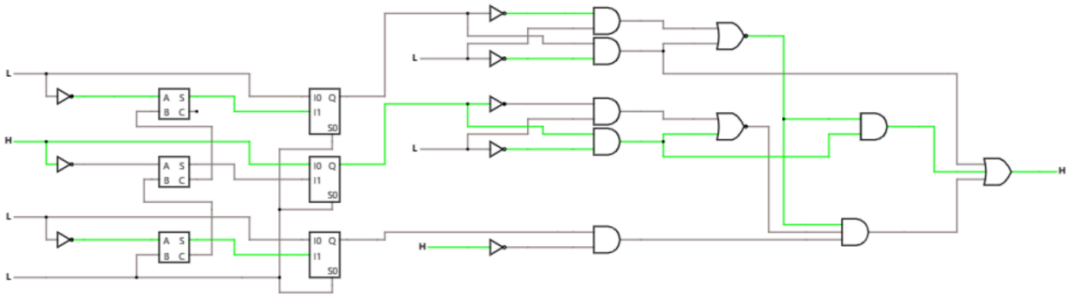

Figure 6. absolute-value detector's internals (Photo/Picture credit: Original).

Furthermore, through software validation, we have found that the designed circuit can correctly achieve the intended logical functions, namely the conversion of absolute values and comparison of numerical magnitudes.

4. Critical path calculation and optimization

This part first focuses on obtaining the minimum delay and corresponding energy on the critical path of a specific circuit structure, and through various optimization methods, achieves a minimum delay that satisfies 1.5 times the original minimum delay, while minimizing energy consumption. Secondly, it further extends the use of PTL (Pass-Transistor Logic) structure to modify the original circuit topology, reducing the number of transistors used, thereby fundamentally reducing both delay and energy consumption.

4.1. Delay model and calculation

Based on the circuit topology determined in Section 3, the delay model, namely the critical path, is illustrated in figure 7.

DOI: 10.54254/2755-2721/39/20230596

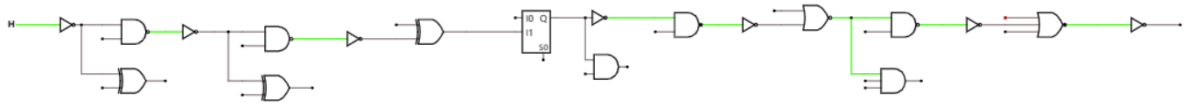

Figure 7. The critical path of our design (Photo/Picture credit: Original).

In this design, the delay of the critical path passes through a 15-level gate circuit. The specified unit inverter sizes are Wn = 430mm, Wp = 650mm, Lp = Ln = 100mm. According to equations below, the g, p, and b parameters for each gate level can be listed as shown in Table 3.

Table 3. Specifics in circuit design.

stage	gate	g	p	b
1	INV	1	1	1
2	NAND	1.398	2	2.43
3	INV	1	1	2.43
4	NAND	1.398	2	1
5	INV	1	1	1
6	XOR	4	4	1
7	2-1 Multiplexer	2.24	6	1
8	INV	1	1	1
9	NAND	1.398	2	1
10	INV	1	1	1
11	NOR	1.6	2	1
12	NAND	1.398	2	2.28
13	INV	1	1	1
14	3-input NOR	2.2	3	1
15	INV	1	1	1

Therefore, the calculation yields:

$$G = g_1 \times g_2 \times g_3 \times \cdots \times g_{15} = 114.08 \tag{5}$$

$$P = p_1 + p_2 + p_3 + \cdots + p_{15} = 30 \tag{6}$$

$$B = b_1 \times b_2 \times b_3 \times \cdots \times b_{15} = 35 \tag{7}$$

$$f = F^{\frac{1}{15}} = (GBP)^{\frac{1}{15}} = 2.071 \tag{8}$$

Based on the obtained parameters mentioned above, we can calculate the minimum delay of the critical path as follows:

$$D_{min} = P + N \times f = 61.065 \tag{9}$$

When calculating the total energy, it is necessary to consider the transition probability of each level from 0 to 1 and from 1 to 0, as well as the load capacitance of each level. In this design, the final load $C_L = 32$ and the probability $\alpha_{0\to1}$ and load capacitance of each level C_L are shown in Table 4.

$$C_L = C_i + C_{i+1} + C_{branch} \tag{10}$$

DOI: 10.54254/2755-2721/39/20230596

Table 4. $\alpha_{0\to1}$ and C_L.

stage	$\alpha_{0\to1}$	C_L
1	0.250	2.815
2	0.188	4.509
3	0.188	8.269
4	0.109	9.049
5	0.109	10.665
6	0.250	10.914
7	0.250	7.576
8	0.250	6.908
9	0.250	7.592
10	0.188	13.953
11	0.188	21.614
12	0.249	20.118
13	0.249	24.33
14	0.250	31.861
15	0.250	47.451

According to the parameters shown in Table 4-2, we can obtain the following results at the given time $V_{DD} = 1V$:

$$E_{tot} = \alpha \times C_L \times V_{DD}^2 = 51.061 \tag{11}$$

4.2. Delay optimization

After determining the minimum delay and energy, it is necessary to optimize the parameters so that the delay is 1.5 times the minimum delay while minimizing the total energy. In this section, two types of optimization methods are mainly employed: one is to change the sizing and fanout values without altering the circuit structure to modify the delay; the other method is to use PTL (Pass-Transistor Logic) instead of CMOS (Complementary Metal-Oxide-Semiconductor) logic to construct a 2-1 multiplexer, thereby reducing the original minimum delay and energy consumption.

4.2.1. Only changing V_{DD}.

After calculating the minimum delay of the critical path for the given circuit topology as 61.065, we can determine that the desired 1.5 times delay is 91.598. According to the formula (12), (13) for the delay of the critical path, it can be observed that the delay is related to V_{DD}:

$$\tau = k \times \frac{V_{DD}}{(V_{DD}-V_T)^2} \tag{12}$$

$$\tau_{opt} = 1.5\tau_{min} \tag{13}$$

Therefore, based on the proportional relationship, we can obtain the equation:

$$\frac{\frac{V'_{DD}}{(V'_{DD}-V_T)^2}}{\frac{V_{DD}}{(V_{DD}-V_T)^2}} = \frac{\tau_{opt}}{\tau_{min}} \tag{14}$$

In this equation $V_{DD} = 1V, V_T = 0.2V$, when we substitute the values and only modify the V_{DD}, we can obtain that when $V_{DD} = 0.776V$, the delay becomes 1.5 times the minimum delay, and the total energy at this point is 30.985.

DOI: 10.54254/2755-2721/39/20230596

4.2.2. Only changing sizing

When changing the sizing while keeping the $V_{DD} = 1V$ unchanged, Excel Solver can be used as a solving tool. The size of each gate in each level is treated as a variable parameter. By utilizing the delay of each gate circuit $d = g \times h + p \times \gamma$, the delay of each level d can be obtained, and thus the overall delay D_{tot} can be determined. The constraints include the condition $D_{tot} = 1.5D_{min}$ that sizing should be between 1 and 2, as well as the constraint.

From this, it can obtain the comparison between the sizing of each level obtained from the final solution and the original sizing, as shown in Table 5.

Table 5. sizing of each gate.

stage	Sizing(new)	Sizing(original)
1	1	1
2	1	1.815
3	1	2.694
4	1	5.575
5	1	3.474
6	1	7.191
7	3.386	3.723
8	1	3.853
9	1	3.055
10	1	4.537
11	1	9.416
12	1	12.198
13	1	7.92
14	1	16.41
15	1	15.451

At this point, the requirement of delay being 1.5 times the minimum delay is satisfied, and the total energy is 15.375.

4.2.3. Changing V_{DD} and sizing

Through the two sections where only the V_{DD} or sizing is changed, we can determine the lower bounds for changing V_{DD} and changing sizing. This means that when combining both optimizations, the adjustment range cannot exceed the numerical range achieved by individual changes. By changing both V_{DD} and sizing, the optimal solution for delay and energy can be achieved. Assuming we first adjust the sizing to achieve a delay that is 1.2 times the minimum delay, using Excel Solver reveals changes in sizing. The updated sizing is shown in the table 6 below.

Table 6. Sizing when changing both V_{DD} and sizing.

stage	Sizing(new)	Sizing(original)
1	1	1
2	1	1.815
3	1	2.694
4	1	5.575
5	1	3.474
6	1	7.191
7	1	3.723
8	1	3.853

DOI: 10.54254/2755-2721/39/20230596

Table 6. (continued).

9	1	3.055
10	1	4.537
11	1	9.416
12	1	12.198
13	1	7.92
14	1	16.41
15	1.569	15.451

At this point, the delay is $D = 1.2D_{min} = 61.065$, and the energy is 14.467. To satisfy the 1.5 times delay requirement by adjusting, since the relationship between the delay and V_{DD} has been explained in the previous section, the calculation formula is as follows:

$$\frac{\frac{V_{DD}}{(V_{DD}-V_T)^2}}{\frac{1}{(1-0.2)^2}} = \frac{1.5}{1.2} \tag{15}$$

The final calculation result is obtained as $V_{DD} = 0.8658V$, and the energy at this point is 10.8446. The entire optimization process can be illustrated as shown in the figure 8.

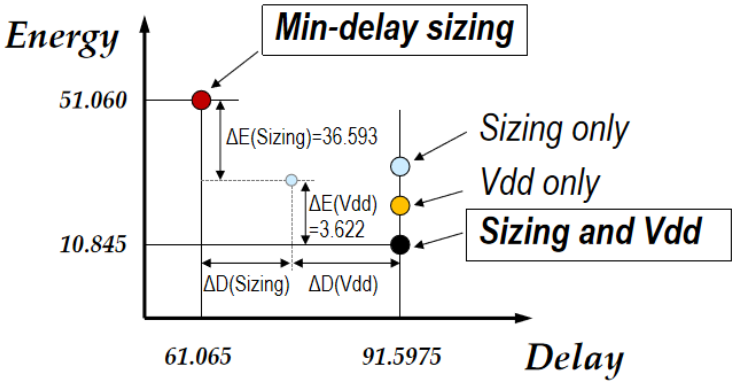

Figure 8. Optimization of V_{DD} and sizing (Photo/Picture credit: Original).

4.3. Using PTL logic

Although CMOS logic can eliminate threshold voltage loss to achieve full swing, it requires a larger number of transistors, resulting in increased delay and energy consumption. On the other hand, PTL logic allows bidirectional transmission, which effectively reduces the number of transistors and fundamentally reduces the total energy and minimum delay.

Specifically, in the circuit design, the 2-1 multiplexer that was originally implemented using CMOS technology is replaced with PTL logic. The specific circuit structure is shown in figure 9.

DOI: 10.54254/2755-2721/39/20230596

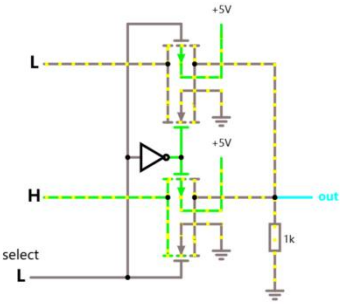

Figure 9. 2-1 multiplexer using PTL (Photo/Picture credit: Original).

In the calculation of the g and p parameters for PTL logic, it is necessary to backtrack and find the path to either V_{DD} or GND. Therefore, the 2-1 multiplexer can be considered with the preceding XOR gate. As a result, the number of stages N is reduced from the original 15 to 14. In PTL logic, the width-to-length ratio of NMOS and PMOS transistors are equal. In this design, we take $W_P = W_n = 430$mm. The newly added XOR gate and the overall structure of the 2-1 multiplexer have g = 4,$p = \frac{4.3\times4}{10.8} + 4 = 5.593$.

Based on this, it can calculate the values of G, P, and f parameters for different circuit topologies:

$$G = g_1 \times g_2 \times g_3 \times \cdots \times g_{14} = 50.929 \tag{16}$$

$$P = p_1 + p_2 + p_3 + \cdots + p_{15} = 25.593 \tag{17}$$

$$B = b_1 \times b_2 \times b_3 \times \cdots \times b_{15} = 35 \tag{18}$$

$$f = \sqrt[14]{F} = \sqrt[14]{GBP} = 2.152 \tag{19}$$

Due to the changes in the parameters D_{min},E_{tot} , and h are also correspondingly altered. As a result, we can obtain the final minimum delay and the modified energy as follows:

$$D_{min} = P + N \times f = 55.721 \tag{20}$$

$$E_{tot} = \alpha \times C_L \times V_{DD}^2 = 43.238 \tag{21}$$

Through the calculations, it can be observed that using the PTL structure can reduce delay and energy consumption. Therefore, if this structure is considered for use in very large-scale integrated circuits (VLSI), it can significantly reduce energy consumption and delay losses.

5. Conclusion

This paper provides a primary exposition on the design and optimization of a 4-bit absolute value comparator. Taking into consideration the requirements of delay, energy, and size in encrypted communication, the article explores four distinct methods to optimize the performance after establishing the circuit's fundamental structure and topology. Through the four optimization methods mentioned above, it can be observed that the PTL structure, due to its alteration of the circuit's topology, fundamentally reduces the delay and energy consumption. When using the method of changing only V_{DD}, the delay meets the requirement of 1.5 times, but the energy does not decrease significantly. When using the method of changing only sizing, there is a noticeable reduction in energy. However, when simultaneously changing both V_{DD} and sizing, the energy reaches its minimum value. Therefore, simultaneously changing V_{DD} and sizing is the optimal method.

Regarding the directions for further optimization, there are currently two main approaches that focus on optimizing the transistor itself. One approach involves altering the width-to-length ratio of MOS transistors. Since the width-to-length ratio affects the on-resistance and parasitic capacitance, it will inevitably impact both delay and energy consumption. The other approach involves modifying the material of the conventional MOS transistors by using a semiconductor material called GaN. GaN offers

DOI: 10.54254/2755-2721/39/20230596

excellent optical characteristics and higher carrier mobility, which can effectively reduce delay by increasing I_{DS}. Therefore, in future research, changing the width-to-length ratio and exploring alternative materials are promising directions for improvement.

References

[1] Venkatesh, S., Lu, X., Saeidi, H., & Sengupta, K. (2020). A high-speed programmable and scalable terahertz holographic metasurface based on tiled CMOS chips. Nature Electronics, 3(12), 785–793.

[2] M. Altuve and N. F. Monroy, "Hidden Markov model-based heartbeat detector using electrocardiogram and arterial pressure signals," Biomedical Engineering Letters, vol. 11, no. 3, pp. 249–261, Jun. 2021.

[3] J. Ge, J. Yang and C. Zhao, "A 1.17ns FO4(1V) Low Energy Cost 4-Bit Absolute-Value Detector," 2021 International Conference on Electronic Information Engineering and Computer Science (EIECS), Changchun, China, 2021, pp. 985-993.

[4] Z. Huang, "Performance Optimization of 4-bit Absolute Value Detector Based on Structural Design You may also like Topologically preserved registration of 3D CT images with deep networks Modeling the Thermal Behavior of a Lithium-Ion Battery Module for Hybrid Electric Vehicle Applications Development of physics module SMA/MA integrated character values based on discovery learning models with approach science process skills Performance Optimization of 4-bit Absolute Value Detector Based on Structural Design," Journal of Physics: Conference Series PAPER • OPEN ACCESS Journal of Physics: Conference Series, vol. 2435, p. 12010, 2023.

[5] Y. Jia, "Design and Optimization of 4-bit Absolute-value Detector Based on CMOS," Journal of Physics: Conference Series, vol. 2435, no. 1, p. 012011, Feb. 2023.

[6] J. Rissman, T. E. Chow, N. Reggente, and A. D. Wagner, "Decoding fMRI Signatures of Real-world Autobiographical Memory Retrieval," J. Cogn. Neurosci., vol. 28, no. 4, pp. 604-620, 2016.

[7] T. Yang, Y. Zhang, S. Xiao and Y. Zhao, "Digital signature based on ISRSAC," in China Communications, vol. 18, no. 1, pp. 161-168, Jan. 2021.

[8] Zemin Zhong. "Oblivious Signature based on Blind Signature and Zero-Knowledge Set Membership," 2021 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), Hualien City, Taiwan, 2021, pp. 1-2.

[9] A. Sengupta, E. R. Kumar and N. P. Chandra, "Embedding Digital Signature Using Encrypted-Hashing for Protection of DSP Cores in CE," in IEEE Transactions on Consumer Electronics, vol. 65, no. 3, pp. 398-407, Aug. 2019.

[10] C. Pradhan, D. Banerjee, N. Nandy and U. Biswas, "Generating Digital Signature using Facial Landmlark Detection," 2019 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 2019, pp. 0180-0184, doi: 10.1109/ICCSP.2019.8698089.

[11] C. Liu, X. Shen, M. Gao and W. Dai, "CSRF Detection Based on Graph Data Mining," 2020 IEEE 3rd International Conference on Information Systems and Computer Aided Education (ICISCAE), Dalian, China, 2020, pp. 475-480.

[12] S. Wang, C. Ni, J. Wang and C. Nie, "Detecting and Defending CSRF at API-Level," 2022 IEEE International Symposium on Software Reliability Engineering Workshops (ISSREW), Charlotte, NC, USA, 2022, pp. 75-80.