Proceedings of the 2023 International Conference on Machine Learning and Automation
DOI: 10.54254/2755-2721/39/20230603

Optimization and application of numerical comparators in autonomous driving technology

Wentao Zhu

College of Information Science and Engineering, China University of Petroleum, Beijing, 102249, China

2019011098@student.cup.edu.cn

Abstract. As one of the hot spots in the field of science and technology in recent years, autonomous driving technology is developing rapidly and arousing wide attention. This study explores the application of numerical comparators in autonomous driving technology, with a particular focus on their potential role in environmental perception and decision-making. We have designed and optimized a 4-bit absolute comparator to address the increasing control requirements and energy optimization goals of autonomous vehicles. The results show that numerical comparators play an important role in autonomous driving technology and can be used to quickly and accurately compare sensor data with thresholds, helping systems make critical decisions such as obstacle detection and trajectory planning. By optimizing the circuit design, we managed to reduce energy consumption and achieve the goal of low latency. The significance of this research is to fill the knowledge gap about the application of numerical comparators in automatic driving technology and provide a new idea for the performance improvement of automatic driving system. In the future, we can further explore the innovative potential of numerical comparators in autonomous driving technology to achieve safer, smarter, and more efficient autonomous driving technology.

Keywords: Autonomous Driving Technology, Numerical Comparators, Environmental Awareness, Decision-Making, Energy Optimization.

1. Introduction

With the rapid surge in technology, autonomous driving has transcended the realm of science fiction to become a tangible reality. The advent of this technology has wrought a profound transformation upon the landscape of the transportation sector, sparking extensive interest and research. Its potential economic, social, and environmental impacts are progressively coming to the fore, rendering it a vibrant and prominent field of investigation. However, as autonomous driving technology experiences rapid growth and widespread application, numerous technical challenges have come to the forefront. Foremost among these challenges is the highly dynamic and uncertain driving environment. Autonomous driving technology necessitates swift, prudent real-time decision-making within the complex and ever-changing traffic milieu. The specter of system failures or unforeseen contingencies looms large, underscoring the imperative for systems with a high degree of reliability and fault tolerance. This calls for the deployment of intricate redundancy mechanisms and refined algorithms to contend with diverse unforeseen scenarios. This, in turn, places substantial demands on the system's latency and information processing capabilities.

DOI: 10.54254/2755-2721/39/20230603

The growing recognition of the pivotal role of numerical comparators in environmental perception and decision-making is becoming increasingly apparent. As fundamental circuit elements, numerical comparators primarily serve to compare the magnitudes of two input values and generate corresponding outputs. Within the realm of autonomous driving technology, numerical comparators can serve as critical decision-makers, discerning the relationship between environmental data and predefined thresholds.

As the requirements for control and advanced functionalities in autonomous vehicles continue to mount, alongside energy optimization goals, the design of circuits necessitates swifter, more reliable, and energy-efficient structures. Achieving this objective hinges upon parameters such as power consumption and delay, which serve as the crux of electronic device manufacturing. This paper employs static CMOS logic, coupled with pass-transistor logic (PTL) and transmission gate logic (TGL), to devise a hybrid design for a 4-bit absolute value detector that compares input values represented in two's complement format. This approach streamlines the circuit, pinpointing specific logic optimizations, particularly for the absolute value detection function, thereby reducing the number of transistors. The paper draws upon the theory of logical effort to translate the capacitance and resistance of each gate into a ratio with respect to the unit-size inverter. After identifying the critical path, it calculates the overall delay and energy consumption. The research investigates the optimization of circuit delay and energy consumption through the manipulation of transistor sizes and voltage scaling (VDD), striving to attain varying optimization objectives (minimum delay or minimum energy consumption with delay not exceeding 1.5 times the minimum delay).

The significance of studying the application of numerical comparators in autonomous driving technology lies in addressing the current dearth of detailed application and performance evaluations within the existing literature. Thus, the impetus behind this study is to enhance our understanding of the role of numerical comparators in autonomous driving technology and optimize the design of absolute value comparators.

2. The basics of autonomous driving

The fundamentals of autonomous driving technology involve several key aspects, including environmental awareness, decision-making, and control. This section will cover these aspects in detail, emphasizing the importance of environmental awareness and the potential applications of numerical comparators in them.

2.1. Principles of Autonomous Driving Technology

Autonomous driving technology is based on advanced sensors and algorithms that enable vehicles to travel safely and intelligently without the need for human intervention. Key technical principles include environmental awareness, decision-making, and control. The environment awareness phase utilizes a variety of sensors, such as lidar, cameras, and ultrasonic sensors, to obtain detailed information about the vehicle's surroundings. The decision stage analyses sensor data and makes appropriate driving decisions based on traffic rules and path-planning algorithms. The control phase translates decisions into actual vehicle control instructions that control the throttle, brakes, steering wheel, etc., to achieve the vehicle's movement.

2.2. Potential applications of numerical comparators

In autonomous driving technology, the numerical comparator, is the basic digital circuit element, Although it may not be the core research topic, it still plays an important role in some specific application scenarios. Especially in the control and decision-making of autonomous driving systems, the simple and effective comparison function of the numerical comparator makes it a key component of some basic tasks.

DOI: 10.54254/2755-2721/39/20230603

2.2.1. Sensor data processing and status detection

Autonomous driving systems rely on a variety of sensors to obtain information about the vehicle's surroundings. In these sensors, the numerical comparator can be applied to the sensor data processing and state detection, so as to help the system to make basic decisions and decisions.

Sensors such as cameras, LiDAR, ultrasonic sensors, etc., return a large number of analog or digital signals. A numerical comparator can be used to process these signals, comparing them to a preset threshold to determine if a particular situation exists. For example, in autonomous driving, a vehicle may need to recognize signs on the road, and a numerical comparator can compare the image-processed signal with a preset threshold to determine whether a particular sign is present. In addition, after the signal collection, the data is processed by the internal computer system, which is mainly divided into three categories: data information, state information, and control information, different interface information is transmitted with different port addresses, of which the optional port address decoding method often uses the digital comparator 74LS688 to form a switching decoding circuit [1].

2.2.2. Obstacle detection and safe distance determination

Obstacle detection is a key task in autonomous driving, which involves judging the distance between the vehicle and obstacles to ensure safe driving. The numerical comparator can play a role in obstacle detection by comparing the distance data returned by the sensor with the preset safe distance threshold to determine whether there is a dangerous approach to the obstacle.

An ultrasonic sensor, for example, calculates distance by sending an ultrasonic pulse and measuring the reverberation time. The measured distance data is entered into a numerical comparator and compared with a preset safe distance threshold. Based on the results of the comparison, the absolute value comparator generates a digital logic signal indicating whether emergency braking or obstacle avoidance measures are required to ensure a safe distance between the vehicle and the obstacle.

Different from the traditional assisted driving technology, the development goal of modern autonomous driving is to achieve complete unmanned control [2]. The detection method based on 3D vision can make the computer detect road conditions more comprehensively. Therefore, in addition to the use of sensors, image processing algorithms paired with cameras are also an important research direction of autonomous driving technology. The detection method based on 3D vision enables the computer to detect the road condition more comprehensively, and the Census transform includes the data comparison module for comparing the relationship between the size of the center pixel [3]. In order to realize the fast response of image modeling, the response delay of the comparator is the key to the whole detection time.

2.2.3. Trajectory planning and position calibration

Trajectory planning is one of the core tasks in the autonomous driving system, which involves how the vehicle travels along the predetermined path to reach the target position. Numerical comparators can assist in position calibration and error correction in trajectory planning.

For example, comparing the current position of the vehicle with a predetermined trajectory can calculate the position error. By entering the position error into the numerical comparator and comparing it with the preset tolerance range, the system can determine whether the vehicle has deviated from the predetermined trajectory. This is often used in the feedback path of automatic control systems. When the sensor returns a control signal, it needs to use a numerical comparator to compare with the input signal to achieve deviation control [4]. This helps the system take timely control measures to adjust the direction of the vehicle and ensure that the vehicle always stays on the predetermined path. In the non-maximum suppression module of the existing SIFT tracking algorithm, the absolute value comparator is also used to provide help for the gradient direction logic implementation of feature points, and the gradient amplitude of alternative feature points is compared with that of neighbouring points in the gradient direction. Alternative feature points located on the edge are detected and removed by local non-maximum suppression, thus eliminating unstable feature points and improving the stability and accuracy of tracking feature points [5].

DOI: 10.54254/2755-2721/39/20230603

3. Numerical comparator design

In this chapter, the structure and optimization process of a 4-bit absolute value comparator will be introduced in detail. This chapter will first outline the goals and requirements of the design, and then describe the circuit topology and logic style adopted. This is followed by critical path optimization and scaling strategies for V_{DD}. Finally, the simulation results are introduced and the performance of the design is evaluated.

3.1. Design goals and requirements

The design goal of this paper is to implement a 4-bit absolute value comparator, which makes the delay as small as possible while fulfilling the basic function of comparing the input value with the threshold size. In order to achieve this goal, this paper mainly starts from two aspects; First, through the basic circuit structure design, the critical path of the whole comparator is shortest; Second, the grid size and the scaling of the power supply voltage of each transistor on the critical path are used as variables to obtain the corresponding curve of delay and energy consumption.

3.2. Circuit topology and logical structure selection

The 4-bit absolute value detector designed in this paper aims at finding the topology with the shortest delay, aiming at the minimum delay of this structure, and making the delay not exceed 1.5 times the minimum delay at the minimum energy. The "delay" here refers to the propagation delay caused by the critical path of the circuit, while the "energy" refers to the total energy extracted from the V_{DD}, including the output load.

The absolute value comparator must have two input signals, one is the threshold known as the criterion of the judgment, and the other is the initial signal of the judgment. The threshold value here is usually positive, so the threshold value is directly entered into the comparison module, and the value to be compared needs to pass through the absolute value module. The structure is as follows in Figure 1.

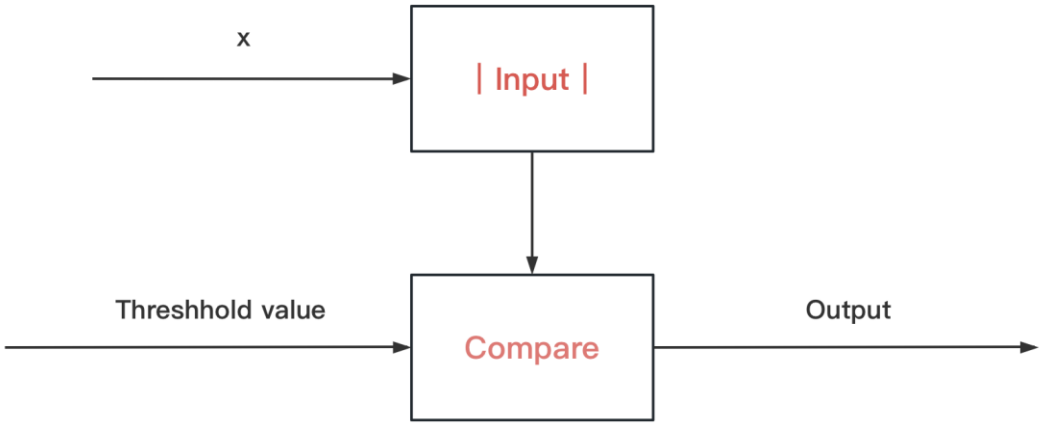

Figure 1. Structure of absolute value detector.

Two designs are used here to compare and reflect the optimization of the topology structure. All of the following structures implement the output "1" when the value to be compared is greater than the threshold. Otherwise, 0 is displayed. The first design principle is to compare the digital bits of the value to be compared with the threshold value respectively, and finally use the symbol bits as the final output judgment value

DOI: 10.54254/2755-2721/39/20230603

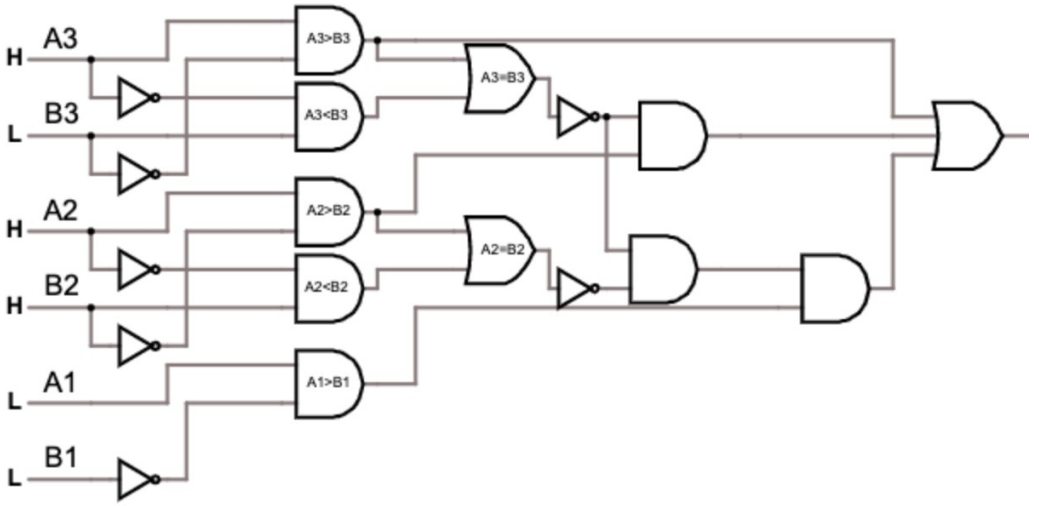

Figure 2. Structure of bit-by-bit compare circuit.

The principle of this design is to compare the size of numerical bits step by step. When the third bit A3 of the value to be compared is greater than the third bit B3 of the threshold value, there is no need to consider the last two bits. In the same way, the higher comparison result is preferred over the lower comparison result output. When comparing the size of the value. At this point, the absolute value comparison has been achieved. Using symbol bit A4 as the final output control can realize the numerical comparison; Since the highest place of the threshold must be 0, when A4 is 0, it is two positive numbers that are comparing sizes. No need to change the results of the previous level; When A4 is 1 and the input value is negative, changing the output of the previous level can compare the size of the whole number.

At the beginning of the design of the second topology, the threshold of the absolute value comparator is set to a variable and compared to a four-digit binary number. In this paper, by using the properties of binary complement, any input value to be compared is transformed into a negative number, and then a positive threshold value is added to the complement of the negative number. Logically, this is the realization of subtraction. At this time, from the logic of the algorithm, the absolute value of the input value is subtracted from the threshold value as a positive number, and the highest bit of the result, that is, the sign bit, can be used as the judging standard for judging the size of the subtraction and the subtraction. If the highest bit (MSB) of the result is 0, it is positive, indicating that the threshold is greater than the input value. If the highest bit (MSB) is 1, the result is negative, indicating that the input value is greater than the threshold.

The addition is the use of full adder, need to consider the problem of carry [6]. The classic multibit full adder uses four full adders in series. As shown below:

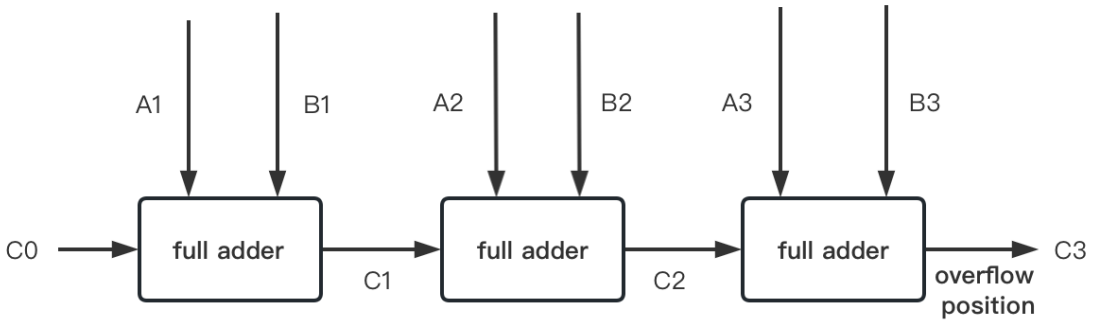

Figure 3. Structure of three-position full adder carry.

DOI: 10.54254/2755-2721/39/20230603

Here, when the fourth digit is added, it must be the case of adding negative and positive numbers, so it only needs to pay attention to whether the third digit carries 0 or 1, and thus a full adder can be reduced. In the multi-bit addition calculation, according to the figure above [7], the calculation formula used is as follows

$$P_i = \overline{A_i}B_i + A_i\overline{B_i} \tag{1}$$

$$G_i = A_iB_i \tag{2}$$

$$C_0 = \overline{A_4} \tag{3}$$

$$C_1 = G_1 + P_1G_0 \tag{4}$$

$$C_2 = G_2 + P_2G_1 + P_2P_1C_0 \tag{5}$$

$$C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1C_0 \tag{6}$$

Another basic structure of the circuit is the use of a data converter consisting of a transmission gate, which logically replaces the absolute value of the module design, and chooses to pass the input directly or pass its complement according to the sign bit (A4), so as to convert positive to negative values [8]. Combined with the above two modules, the circuit structure in the following figure is formed.

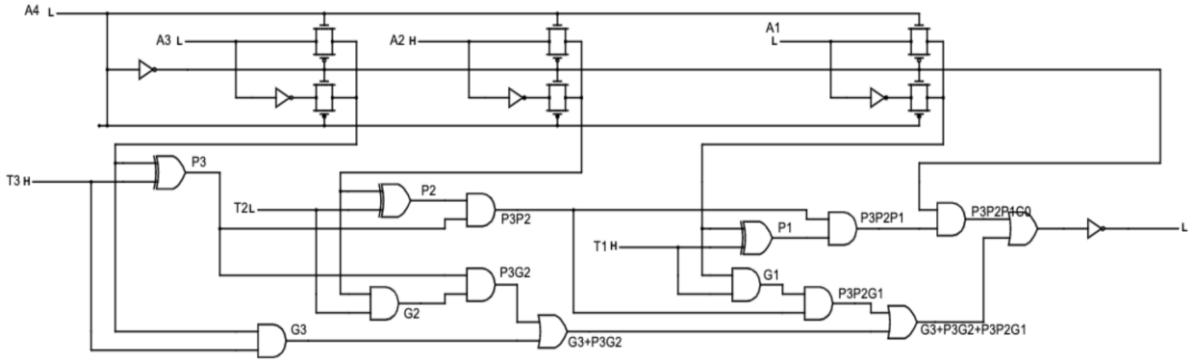

Figure 4. Structure of adder comparison circuit.

From the point of view of the delay of typical logic gates, compared with the first version of the design, the second version of the design shortens the critical path delay, reducing the circuit delay to 10 levels, and the shortest path to 7 levels. In addition, the use of transmission gates as data selectors, rather than traditional XOR gates, reduces the required latency and contributes to the timing optimization of the circuit. However, the complexity of the logic gate circuits in this design makes it difficult to accurately calculate the latency of the critical path. Therefore, the threshold value of 3 is chosen, and the logic expression obtained before is simplified and integrated into a 4 input circuit, making the calculation and optimization process more convenient.

3.3. Critical path delay calculation and V_{DD} scaling

The critical path is the logically longest and highest delay path from input to output in the schematic. In the critical path we designed, as shown in the figure, this is the critical path.

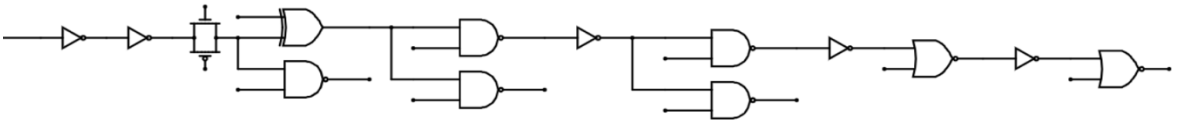

Figure 5. Structure of critical path.

DOI: 10.54254/2755-2721/39/20230603

To calculate the delay of the design, use a logical effort to find the delay. Before calculating the delay, it is necessary to show the calculation results of the logic gate parameters used in this design, as shown in the figure below

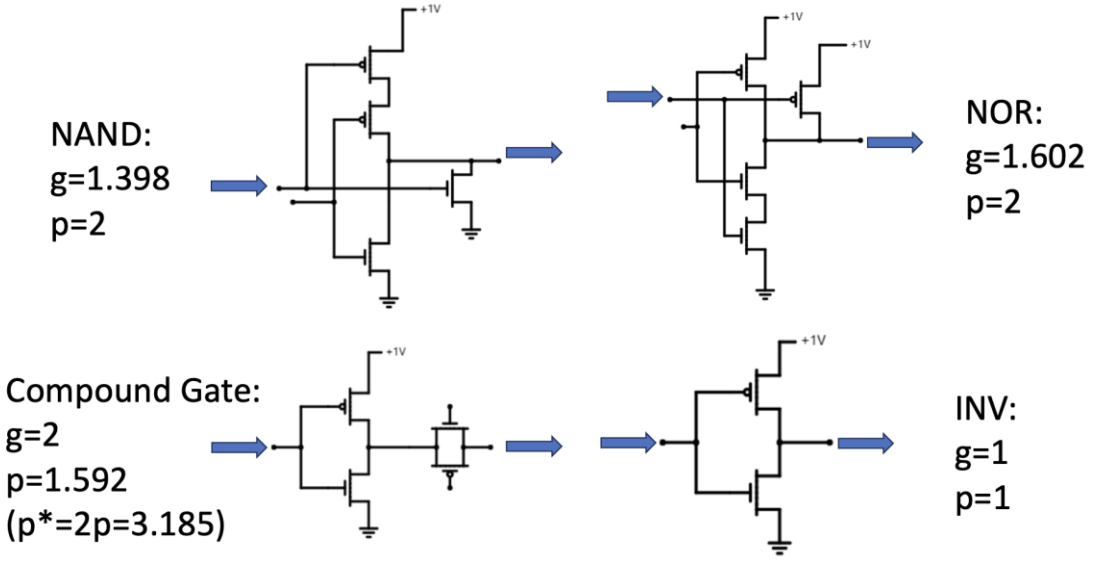

Figure 5. Gate parameter.

The formula for the total delay D is

$$D = \sum d_i = D_F + P \tag{7}$$

$$D_F = \sum f_i \tag{8}$$

$$P = \sum P_i \tag{9}$$

The total delay D is equal to the sum of the stage delay d_i, which is equal to the minimum path effort delay D_F plus the path parasitic delay P.

Path effort delay is the sum of all levels of effort. According to the squared theory, when the product of a set of numbers is constant, the sum of the set of numbers is minimal only if all the numbers are chosen to be equal. In summary, path latency is minimized when all stages in the path have the same effort. Path logic effort is defined as the product of logical effort G, branch effort B, and electrical effort H, as follows:

$$F = GBH \tag{10}$$

$$G = \prod g_i = 1^4 \times 2^2 \times 1.398^2 \times 1.602^2 = 20.063 \tag{11}$$

$$H = \frac{C_{out}}{C_{in}} = 32 \tag{12}$$

$$B = \prod b_i = \frac{2+1.398}{1.398} \times 2 \times 2 = 9.722 \tag{13}$$

$$b_i = \frac{C_{onpath}+C_{offpath}}{C_{onpath}} \tag{14}$$

The critical path path for this design has 10 levels, and with each level set to the same effort, this will result in a more balanced capacitance distribution [9]. the effort f_i is calculated as follows

$$F = GBH = 6241.679 \tag{15}$$

$$f_i = \sqrt[10]{F} = 2.396 \tag{16}$$

DOI: 10.54254/2755-2721/39/20230603

In this case, the path delay is minimized

$$D_{min} = f_i \times N + \sum P = 2.396 \times 10 + 1 \times 4 + 3.185 \times 2 + 2 \times 4 = 42.33 \quad (17)$$

f_i is the size of each stage. N indicates the number of phases.

Changing the size of the gate will affect the total capacitance of the circuit, resulting in a change in the energy consumption of the critical path. As can be seen from the following energy calculation formula, changing the power supply voltage will directly affect the energy consumption. After the minimum delay is obtained, it is clear that the power consumption will not be the optimal state. Reducing V_{DD} can significantly reduce energy consumption. But at the same time, the increase in delay is inevitable.

$$E = C{V_{DD}}^2 \quad (18)$$

The gate size and input V_{DD} are adjusted for each gate level to find a balance between power consumption and delay. This article assumes that $\gamma = 1, V_T = 0.2V$. In addition, the formula for delay proportional to V_{DD} is as follows

$$D \propto \frac{V_{DD}}{(V_{DD} - V_T)^2} \quad (19)$$

Gate delay is

$$t_i = P_i + g_i \times h_i \quad (20)$$

Gate energy consumption is

$$E_i = C_i \times {V_{DD}}^2 \quad (21)$$

$$h_i = \frac{C_{out}}{C_{in}} \quad (22)$$

$$D_{min} = k \frac{V_{DD}}{(V_{DD} - V_T)^2} \quad (23)$$

$$D = D_{gate} + D_{V_{DD}} \quad (24)$$

Based on the previous analysis, it can be known that optimizing the gate size or optimizing the supply voltage can reduce energy consumption without exceeding the delay limit. But this is not optimal, because only one variable is handled in both cases. According to the expression of the energy calculation, both the gate size and the supply voltage affect the energy consumption. Therefore, this article will explore the best state that can be achieved when optimizing both. This article uses Excel Solver as the optimization tool for this design. In the optimization process, the gate size and supply voltage are set as variables, the maximum allowable value of delay is set as constraints, and the target is set as the minimum value of energy consumption. Throughout the calculation process, the formulas for the relevant variables are listed above. The figure below shows the optimized data.

In this design, a margin of 1.5 times minimum delay is selected to give room for size and V_{DD} optimization, and the V_{DD} range in this design is between 0V and 1V. The phase effort with minimum delay is shown in the figure below

DOI: 10.54254/2755-2721/39/20230603

Table 1. Each gate parameter at minimum delay.

	TNV	TG	TG	NAND	INV	NAND	INV	NOR	INV	NOR
stage	1	2	3	4	5	6	7	8	9	10
size	1	1.678	2.01	1.417	1.214	2.908	2.492	5.971	8.93	21.396
g	1	2	2	1.398	1	1.398	1	1.602	1	1.602
p	1	3.185	3.185	2	1	2	1	2	1	2
Branch effort	0	1.398	1.398	1	1.398	0	0	0	0	0
Energy	0.5	1.08755	1.30273	0.64578	0.45525	1.73945	1.22653	2.90383	3.863	11.9788
Delay	3.396	5.581	5.581	4.396	3.396	4.396	3.396	4.396	3.396	4.396
Alpha	0.25	0.25	0.25	0.1875	0.1875	0.24609	0.24609	0.21629	0.21629	0.249
f*	2.396	2.396	2.396	2.396	2.396	2.396	2.396	2.396	2.396	2.396
h	2.396	1.198	1.198	1.71388	2.396	1.71388	2.396	1.49563	2.396	1.49563

Total energy expenditure=25.7029;

Total delay=42.33;

This article uses an Excel solver as a useful optimization tool. In Excel solver, set the minimum energy consumption as the target, set the variables to the size of each gate and V_{DD}, and let go after 1.5 times the minimum delay. The following data is obtained

Table 2. Each gate parameter at 1.5x minimum delay.

	TNV	TG	TG	NAND	INV	NAND	INV	NOR	INV	NOR
stage	1	2	3	4	5	6	7	8	9	10
size	2	1.07908	1.009101	1	1	1.022422	1	1	1.02929	4.822711
g	1	2	2	1.398	1	1.398	1	1.602	1	1.602
p	1	3.185	3.185	2	1	2	1	2	1	2
Branch effort	1	1	1.699	2	1	2	1	1	1	1
Energy	1	0.699378	0.654024	0.45574	0.375	0.611571	0.492188	0.486322	0.445257	2.70005
Delay	1.53954	6.925599	9.919707	5.908808	2.022422	5.823087	2	4.641574	5.685474	19.02879
Alpha	0.25	0.25	0.25	0.1875	0.1875	0.24609	0.24609	0.21629	0.21629	0.249
h	0.53954	1.8703	3.367354	2.796	1.02242	2.734683	1	1.648922	4.685474	10.62971

Total energy expenditure=7.91953;

Total delay=63.495;

From the results in the figure above, we can see that the energy optimization results are still very obvious, and the energy saving of 69% from 25.7 to 7.9 reflects the remarkable effect of optimization.

This paper also calculates the optimization results for the minimum delay of each magnification. Since the V_DD is limited to 0 to 1V, the optimization is basically by the gate size before the 1.5x minimum delay. When the delay scaling is large enough, the optimization effect of V_DD introduced is obviously inferior to that of gate size. When the two variables are given equal priority at the time of setting, the optimizer prioritizes the gate size over V_DD in order to obtain lower power consumption. It also shows that the optimization of gate size is better than V_DD in this design [10].

DOI: 10.54254/2755-2721/39/20230603

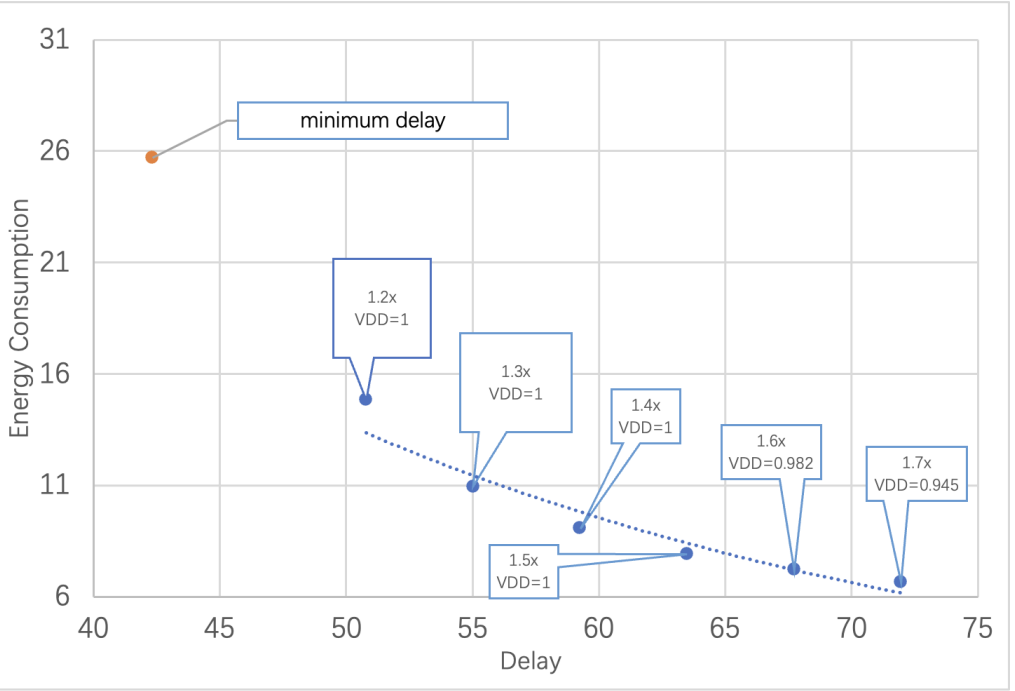

Figure 6. Relationships of D and E under the Best Design.

3.4. Discussion and summary

This section describes how to optimize the critical path. The calculation of all levels of parameters that affect the critical path is determined, and the size of the door is adjusted to achieve the minimum delay. In addition, the strategy of changing the size of the gate and V_{DD} is also considered to achieve the minimization of energy.

In the case of meeting the minimum delay requirements, the energy consumption can be significantly reduced, and the design goal is achieved. Although the design in this paper is for absolute value comparators, the design principles and optimization techniques adopted can have wider applicability in other circuit elements, improving the efficiency and performance of the overall digital system. Through the introduction of this chapter, readers can better understand the design process and results of this paper.

4. Future development

This chapter will explore the application prospects and future directions of numerical comparators in autonomous driving technology, discuss possible innovations, challenges, and solutions, and how to further enhance the role of numerical comparators in autonomous driving.

4.1. Application prospect of numerical comparator in autonomous driving technology

With the rapid development of autonomous driving technology, the number of sensors and processors is increasing, which leads to a large amount of data that needs to be processed and analysed. As a key digital circuit element, the numerical comparator has a wide application prospect in the automatic driving system. It can be used in various decision-making and control aspects, such as obstacle detection, lane keeping, adaptive cruise control, etc. By quickly and precisely comparing sensor data and setting thresholds, numerical comparators can help systems make accurate judgments and decisions.

4.2. Innovation and challenge

As autonomous driving technology evolves, numerical comparators have innovative opportunities and challenges in the following areas:

DOI: 10.54254/2755-2721/39/20230603

With the increasing demand for computational performance in autonomous driving systems, high-performance numerical comparators are becoming particularly important. Designing faster and more accurate comparators to meet the requirements of high-speed data processing is an important innovation point.

Autonomous driving systems need to operate for long periods of time, so low-power design becomes critical. Designing a low-power numerical comparator to extend the battery life of the system while maintaining high performance is a challenging task.

Autonomous driving systems need to work in a variety of complex environments and situations, so the numerical comparator needs to have good robustness and fault tolerance. Designing comparators that can handle noise, jitter, and uncertainty is an area worth exploring.

4.3. Solutions and future directions

To further enhance the role of numerical comparators in autonomous driving, the following solutions and future directions can be considered:

Using deep learning techniques to optimize the performance and energy consumption of numerical comparators, neural networks can be trained to obtain more accurate comparison results. This method can adapt to different data distributions and environments and improve the accuracy of the comparator.

Develop intelligent energy management strategies that dynamically adjust the comparator's operating mode and voltage based on real-time demand to achieve the best balance of energy efficiency and performance. This helps extend the battery life of the system.

The fusion of data from different sensors, and the comparison and judgment on the fused data, can improve the system's understanding of the environment and decision-making ability. Designing numerical comparators adapted to multimodal data fusion is a promising direction.

5. Summary

In the design of an absolute value comparator, two kinds of topologies are given according to two completely different calculation ideas. The analysis of the gate level delay caused by the mechanism makes the design delay of the second full adder shorter. Then the critical path of the second circuit structure is found, and the delay calculation is carried out considering factors such as its branches, gate size, and delay at all levels. Based on the minimum delay, the influence of gate size and V_{DD} on delay and the energy consumption is explored by relaxing the delay constraint conditions. In order to consider the influence of the two factors at the same time, this paper uses Excel Solve as an optimization tool to find the optimization effect of the two variables on the energy consumption level under each multiple delay condition after setting the restriction conditions.

The problem of energy and delay has always been the core pain point in chip design, and the two opposite relationships are doomed to be unable to have the best of both worlds and can only find the most appropriate balance point between the two to meet the needs of different applications. At the same time, numerical comparators as a key component in autonomous driving systems will continue to play an important role in the future. Through continuous innovation and optimization of the circuit structure and individual parameters, we can expect to see higher performance, lower power consumption, and more robust numerical comparators applied in various autonomous driving scenarios, contributing to the realization of safe, intelligent, and efficient autonomous driving technology.

References

[1] Ding Yudong. Dynamic Data Acquisition and Processing System [D]. Chongqing University,2003.

[2] Zhang Xiang. Global Automotive Technology Development Trend in 2013 [J]. Automotive Engineer,2013(03):19-21+52.

[3] Zhu Zeqi. Research and design of embedded 3D industrial camera control System based on binocular vision [D]. Hunan university, 2022. DOI: 10.27135 /, dc nki. Ghudu. 2020.003545.

DOI: 10.54254/2755-2721/39/20230603

Szytula A and Leciejewicz J 1989 Handbook on the Physics and Chemistry of Rare Earths vol 12, ed K A Gschneidner Jr and L Erwin (Amsterdam: Elsevier) p 133

[4] Y. Liu, Y. Wang, Z. Wen and X. Yuan, "Automatic driving path planning based on A-Star algorithm," *2022 7th International Conference on Intelligent Informatics and Biomedical Science (ICIIBMS)*, Nara, Japan, 2022, pp. 19-21, doi: 10.1109/ICIIBMS55689.2022.9971587.

[5] Yang Ying. Research on image processing and tracking algorithm based on PICO384 [D]. Nanjing University of Science and Technology,2017.

[6] A. K. Yadav, B. P. Shrivatava and A. K. Dadoriya, "Low power high speed 1-bit full adder circuit design at 45nm CMOS technology," *2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE)*, Bhopal, India, 2017, pp. 427-432, doi: 10.1109/RISE.2017.8378203.

[7] J. Saini, S. Agarwal and A. Kansal, "Performance, analysis and comparison of digital adders," *2015 International Conference on Advances in Computer Engineering and Applications*, Ghaziabad, India, 2015, pp. 80-83, doi: 10.1109/ICACEA.2015.7164650.

[8] D E Wallace. Digital circuit layout techniques: the US, US6360352 B2[P]. 2002.

[9] Kaveh Shakeri and James D. Meindl. A Compact Delay Model for Series-Connected MOSFETs.Proceedings of the 12th ACM Great Lakes symposium on VLSI, P37-40,2002.

[10] T. Sakurai.CMOS inverter delay and other formulas using alpha -power law MOS model. IEEE International Conference on Computer-Aided Design (ICCAD-89) Digest of Technical Papers,n.d,1988