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A low-latency and energy-efficient 4-bit absolute value detector for brain-machine interface applications

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Abstract. This research article aims to develop a 4-bit absolute value detector, balancing speed and power efficiency, with potential applications in Brain-Machine Interface (BMI) systems. The detector outputs a binary signal, indicating whether the absolute value of the input surpasses a predefined threshold. The design integrates two primary modules: an absolute value calculator and a comparator. Initially, the study focuses on enhancing the architecture of a multiplexer-based adder for absolute value calculation and selecting an efficient comparator structure, emphasizing least significant bit comparison. Further, the implementation of logic gates using Complementary Metal-Oxide-Semiconductor (CMOS) technology is elaborated. The research concludes by assessing the minimum delay achievable in the critical path, quantified at 74.22 units, and investigating strategies to minimize energy consumption. This is achieved by adjusting gate dimensions and supply voltage, aiming for a delay 1.5 times the minimum. The energy expenditure of the critical path is extrapolated to estimate the overall circuit consumption. The findings demonstrate that, at 1.5 times the minimal delay, the circuit achieves a maximum energy savings of 62.8% with a supply voltage of 0.815V.

Keywords: 4-bit absolute value detector, Delay optimization, Energy consumption, BMI, CMOS technology

1. Introduction

Brain-Machine Interface (BMI) stands as a technology with significant potential, which offers hope for restoring physical mobility in individuals afflicted with severe motor impairments resulting from brain injuries, neurological disorders, and limb amputation [1]. One challenge facing BMI technology is the delicate balance between calculation speed and energy consumption [2]. To enhance the efficiency of bioelectrical signal interpretation and facilitate quicker interactions with external devices, a high processing speed is required, leading to increased electrical energy consumption. However, due to the need for long-term and portable operation of implanted brain terminals, careful control of energy usage is imperative. Implanted brain terminals cannot consume much energy, as it would be powered by a battery, or even bioelectricity [3]. The basic structure of a computational circuit includes an abs-value detector. Therefore, researching the balance between the calculation speed and energy consumption of the abs-value detector is crucial for BMI technology.

This research focuses on a low-delay design of a 4-bit abs-value detector and its optimization. First, the paper introduces the design of the 4-bit abs-value detector in chapter 2. This part includes the

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choice with minimal delay between its different possible structures, and optimization of chosen structure. It also shows how to implement the structure with CMOS. In chapter 3, the paper calculates the minimal practical delay and corresponding energy of the structure by gate sizing and adjusting V_{dd} of the circuit. And estimates the minimal possible energy for the circuit at 1.5 times of minimal delay by 3 ways: gate sizing, adjusting V_{dd} and both. It aims to provide assistance in further improving the processing speed and battery life of current BMI brain-implanted terminals, which would be helpful for the patients suffering from brain injuries.

2. Structure of the abs-value detector and optimization

2.1. Basic logic of abs-value detector

The 4-bit abs-value detector consists of 2 parts: abs-value calculator and comparator [4]. The input x[n] is passed through abs-value calculator, and its absolute value would be input into comparator, compared with the threshold value. If the abs-value of the input exceeds a threshold, then the output would be logical "1", and otherwise the output would be "0". Process shown in figure 1.

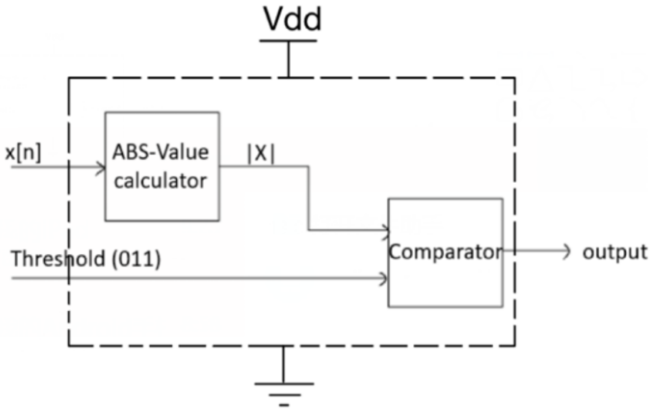

Figure 1. Overall structure of the 4-bit abs-value detector [4]

In this research, the threshold chosen for energy calculation is 011(3), but the comparator can compare the input value with other 3-bit input thresholds as well.

The supplied voltage used for the circuit in this project is limited to $V_{dd} \in (0, 1]$V. The whole circuit is implemented by CMOS logic. The input is assumed to be a 4-bit, 2's complement format number which comes from a chain of unit inverter. The output bit is connected to a loading capacitance C_L, which is 32 times of the capacitance if a unit-sized inverter. The unit-sized inverter used for this research has parameter as follows: $Wp = 650\text{nm}, Wn = 430\text{nm}, Lp = Ln = 100\text{nm}, V_{th} = 0.2\text{V}$.

2.2. Structure of abs-value calculator and optimization

The abs-value calculator can be implemented MUX-based adder [5]. Shown in figure 2: Bit A3 determines the sign of the input. If A3 is 0, the input is equal to or larger than 0, then other bits would pass the MUX directly. If A3 is 1, the input is negative, then the circuit would flip other bits and pass them to an adder. For any binary number, its opposite number would be its bit flipped number + 1. Then the result of adder would be passed through MUX.

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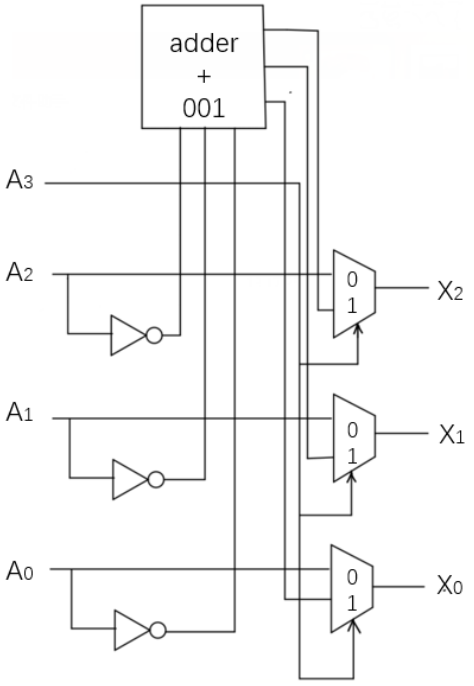

Figure 2. Overall logic of MUX-based adder abs-value calculator (Photo/Picture credit: Original)

To minimize the delay and power utilization of the circuit, the structure of the circuit should be as simple as possible. The calculation process of the adder is illustrated in figure 3.

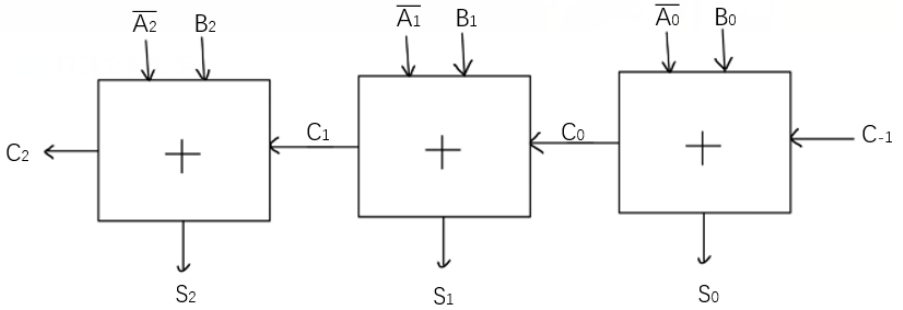

Figure 3. Overall internal configuration of a 3-bit adder (Photo/Picture credit: Original)

To calculate the opposite number, input B2, B1, C-1 is always 0, and B0 is always 1. So, the structure can be simplified to figure 4.

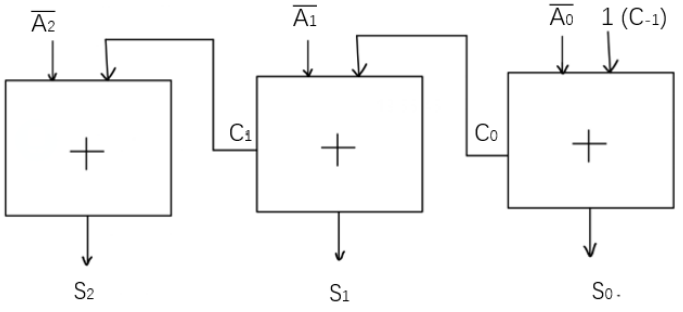

Figure 4. Simplified structure of a 3-bit adder (Photo/Picture credit: Original)

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Instead of 3 full adders, the simplified structure can be implemented with 3 half-adders. For each half-adder, the truth table is as follows in table 1.

Table 1. Half-adder truth table

$\overline{A_i}$	C_{i-1}	C_i	S_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Based on that, the logic equation for each bit shown in the figure are $C_0 = \overline{A_0}$, $C_1 = \overline{A_1}$ AND C_0, $S_0 = A_0$, $S_1 = \overline{A_1}$ XOR C_0, $S_2 = \overline{A_2}$ XOR C_1. The overall circuit for the adder is illustrated in figure 5.

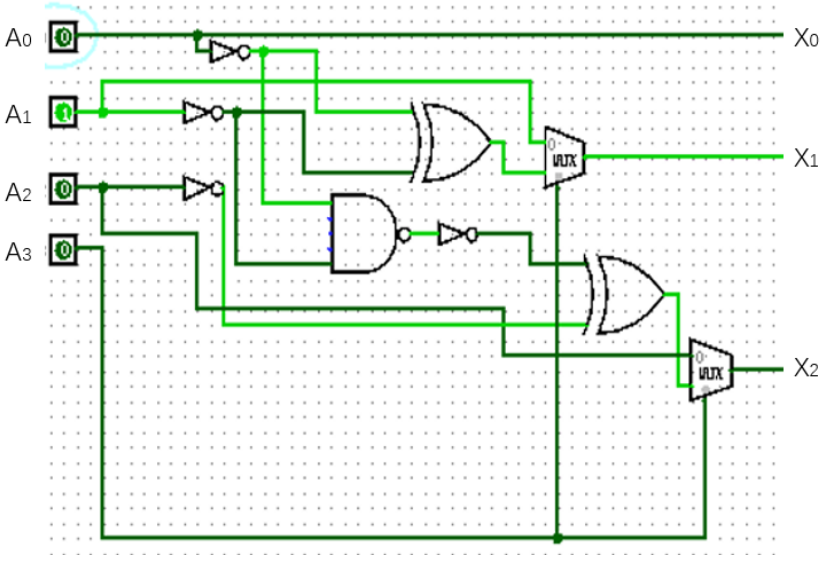

Figure 5. Detailed configuration of a 3-bit adder (Photo/Picture credit: Original)

2.3. Structure of comparator and optimization

The comparator for the circuit is chosen between two types of 3-bit comparators: Starting from LSB (Least Significant Bit) to MSB (Most Significant Bit) (called type I in following passages) and starting from MSB to LSB (called type II). The structures are shown in figure 6.

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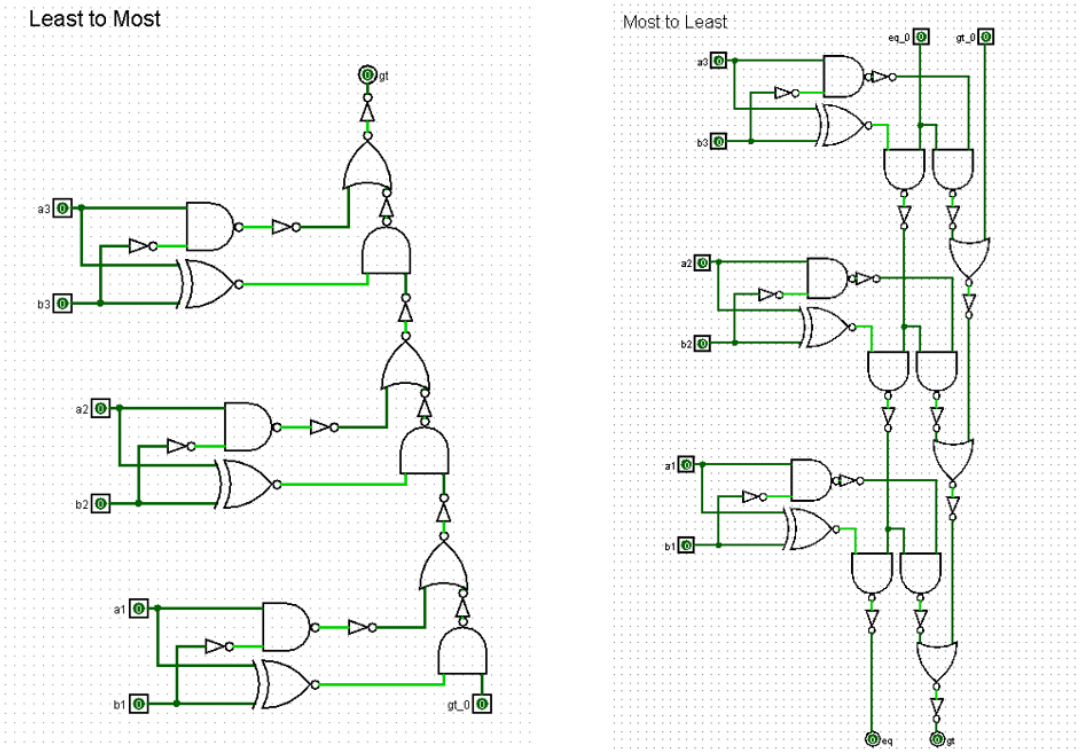

Figure 6. Two types of comparators, with Type I displayed on the left and Type II on the right (Photo/Picture credit: Original)

The type I comparator is chosen for the circuit, and there are two reasons: 1. The type I comparator consists of less gates, and thus would save energy. 2. The order of previous signal outputting from abs-value calculator is from LSB to MSB, so LSB can be processed by the comparator first, and decrease overall delay. Finally, after linking different parts of the abs-value detector, the overall circuit diagram is illustrated below in figure 7.

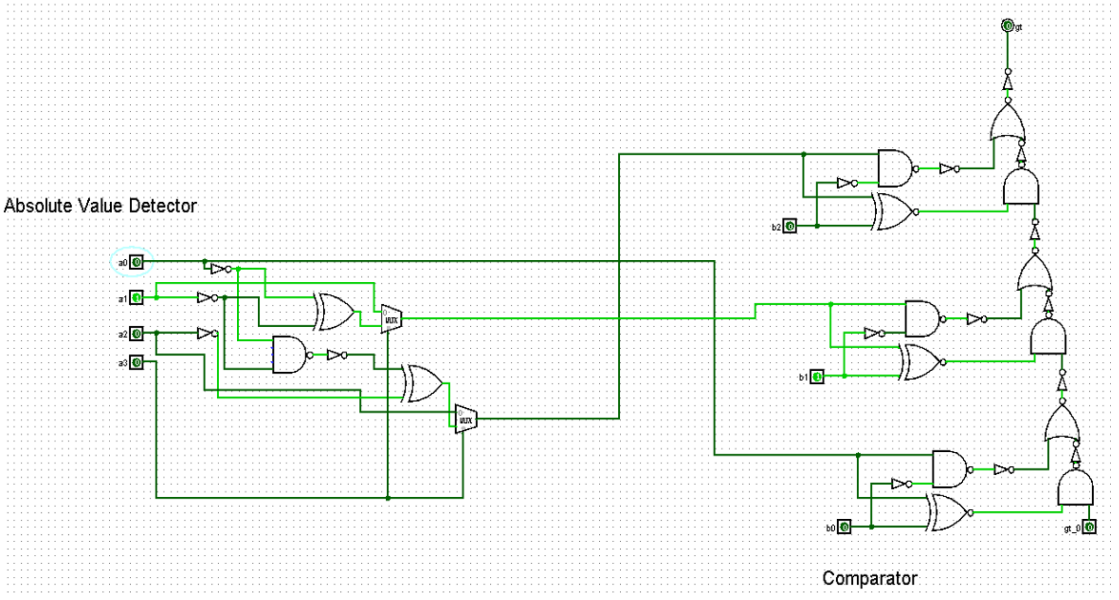

Figure 7. Overall circuit diagram (Photo/Picture credit: Original)

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2.4. Implementation of gates and MUX with CMOS

Compared to international technology roadmap of semiconductors (ITRS), CMOS technology is superior in terms of both delay and energy consumption [6]. Five types of gates are needs to implement the designed circuit: inverter, 2-NAND, 2-NOR, 2-XOR and 2-MUX. The unit-sized inverter used for this reach has parameter as follows: $Wp = 650nm, Wn = 430nm, Lp = Ln = 100nm$. Thus, Wp and Wn is roughly 1.5: 1.

To determine the circuit's delay, the g-factor h-factor and p-factor are needed for each gate implemented with CMOS.

$$g = \frac{R_{gate} \cdot C_{in,gate}}{R_{inv} \cdot C_{in,inv}} \tag{1}$$

$$p = \frac{C_{par,gate}}{C_{par,inv}} \tag{2}$$

For each gate, the structure implemented by CMOS is shown below in figure 8.

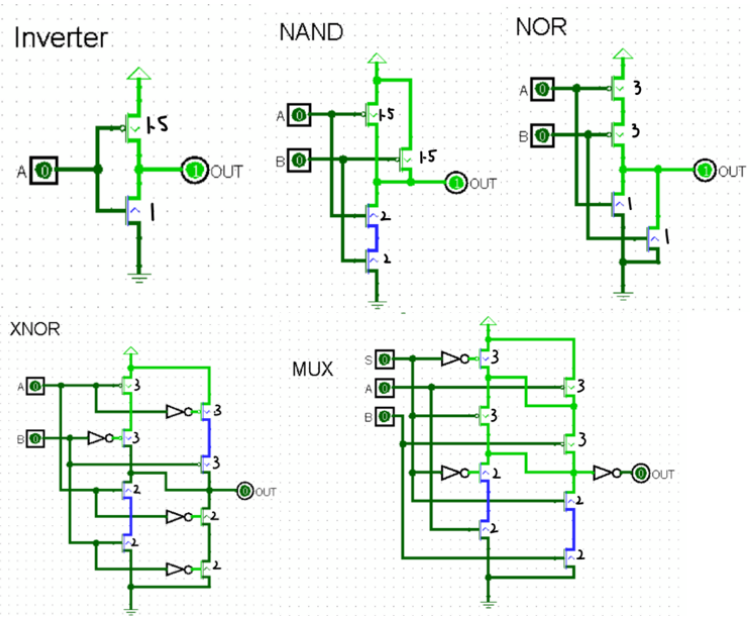

Figure 8. CMOS implementation of gates (Photo/Picture credit: Original)

Based on equation (1) and (2), the g and h parameters are as follows (assume $R_{gate} = R_{inv}$) in table 2 [7, 8].

Table 2. g, h factors of gates

Gate	g	h
NOT (unit inverter)	1	1
NAND	$\frac{1.5+2}{2.5} = 1.4$	$\frac{1.5+1.5+2}{2.5} = 2$
NOR	$\frac{3+1}{2.5} = 1.6$	$\frac{3+1+1}{2.5} = 2$
XOR	$\frac{3+3+2+2}{2.5} = 4$	$\frac{3+3+2+2}{2.5} = 4$
MUX	$\frac{1}{3} \cdot \left(\frac{3+3+2+2}{2.5} + \frac{2+3}{2.5} + \frac{2+3}{2.5}\right) = \frac{8}{3}$	$\frac{3+3+2+2}{2.5} = 4$

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3. Calculation of critical path of minimal energy of 1.5×minimal delay.

The next step is to calculate the possible minimal energy of the circuit when it has a delay of 1.5×minimal delay.

3.1. Assumptions for the circuit calculations

To simplify the calculation, here are two assumptions for the calculation process. (a) In this study, it is assumed that all gates on the same stage have the same size as the corresponding gate on the critical path, so that none of the non-critical path would have a longer delay than the critical path. (b) Based on assumption (a), the total energy of the whole circuit is assumed to be proportional to the critical path's energy.

Assumption (b) is grounded in the following rationale:

The formular for energy calculation is:

$$E = \sum \alpha_i \cdot C_i \cdot V_{dd}^2 \tag{3}$$

α_i is possibility of an input to change from 0 to 1, $\alpha_i = P_0 \cdot P_1$ [9]. Thus, based on assumption (a), the ratio of total energy consumption and energy consumption of the gate on the critical path for each stage is:

$$k_i = \frac{\sum \alpha_i \cdot g_i}{g_{on\ path}} \tag{4}$$

The g_i and $g_{on\ path}$ is settled for the circuit. So, it is reasonable to take the average of k_i to get the ratio of total power usage of the entire detector and the critical path's power usage.

3.2. Calculation of minimal delay and corresponding critical path's energy

3.2.1. Minimal delay of critical path. The method to estimate the delay of the entire detector is to calculate the critical path's delay [10]. The critical path of the circuit designed is illustrated in figure 9. The inverter at the beginning is a size-1 inverter since the input signal is from a chain of size-1 inverters. The last capacitor is C_L which is 32 unit-sized inverters.

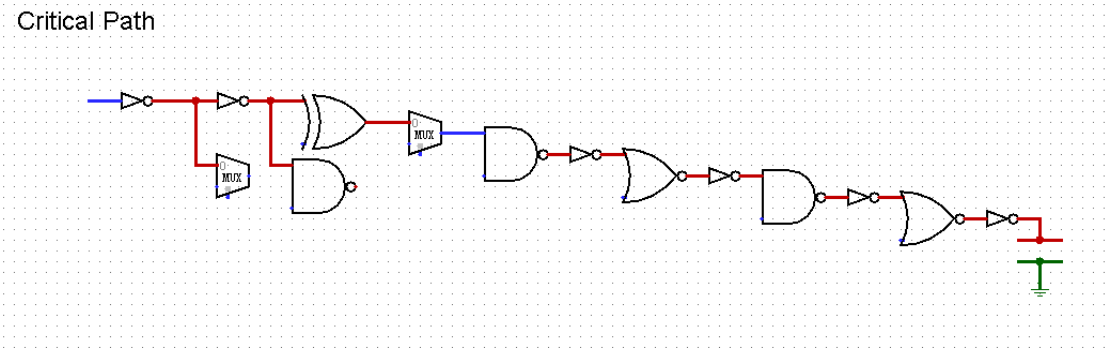

Figure 9. Critical path topology (Photo/Picture credit: Original)

The formular for the delay is:

$$D = (\sum(g_i \cdot h_i \cdot b_i + p_i)) \cdot \frac{V_{dd}}{(V_{dd} - V_{th})^2} \tag{5}$$

$$h = \frac{C_{out}}{C_{in,gate}} = \frac{C_{i+1}}{C_i} \tag{6}$$

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$$b = \frac{C_{onpath} + C_{branch}}{C_{onpath}} \tag{7}$$

For $V_{dd} \in (0, 1]$V, the $\frac{V_{dd}}{(V_{dd}-V_{th})^2}$ term is monotonic increasing. So, for minimal delay, choose V_{dd} = 1V.

For the whole critical path, C_{in} = 1 (unit-sized inverter) and C_{out} is 32 (CL). Thus, $H = \prod h_i = 32$. There are two branches on the critical path, and based on assumption (a), $B = \prod b_i = 4.95$. And $G = \prod g_i = 53.52$. To get the minimal D, introduce a new parameter f:

$$f = g_i \cdot h_i \cdot b_i \tag{8}$$

For minimal D, use mean value inequality, corresponding f^*:

$$f^* = \sqrt[N]{G \cdot B \cdot H} \tag{9}$$

Here, N represents the quantity of gates along the path.

With equation (1) (2) (5) ~ (9), for the critical path, the corresponding minimal delay and gate size is shown in table 3.

Table 3. Sizes of gates when f^* = 2.125

	C_1	C_2	C_3	C_4	C_5	C_6	
Gate size	1	0.5795	0.9122	0.4846	0.3862	0.5861	
	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_L
Gate size	1.2456	1.6543	3.5153	5.3357	11.3384	15.0588	32

And the possible minimal delay for this circuit is: $D = 74.22$ unit. The 1.5 times of minimal delay is: $D_{1.5} = 111.33$ unit

3.2.2. Energy of critical path under minimal delay. According to equation (3), α_i is needed to calculate the energy of critical path. α_i is possibility of an input to change from 0 to 1 in one clock cycle, $\alpha_i = P_0 \cdot P_1$ [9].

For the circuit designed in this research, the input is considered a random 4-bit 2's complement number, and threshold is 011. Based on that, values of α_i are as follows in table 4.

Table 4. factor α_i for each load when threshold is 011

α_1	α_2	α_3	α_4	α_5	α_6	
0.25	0.25	0.25	0.25	0	0	
α_7	α_8	α_9	α_{10}	α_{11}	α_{12}	α_L
0.1875	0.1875	0.2344	0.2344	0.2148	0.2148	0.2148

And energy of critical path under minimal delay $E = 15.9085$ unit

3.3. Minimizing energy consumption at 1.5×minimal delay by resizing gates and adjusting V_{dd}

3.3.1. Predictions about relationship between V_{dd} and E_{min}. In equation (5), the terms of V_{dd} and gate size are separate. Thus, it is reasonable to consider V_{dd} only and find the possible range of V_{dd} at first. To achieve 1.5×minimal delay by only adjusting V_{dd}, it should satisfy the equation:

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$$\frac{V_{dd_{min}}}{\left(V_{dd_{min}} - V_{th}\right)^2} = 1.5 \times \frac{1}{(1-0.2)^2} \tag{10}$$

And corresponding V_{dd_min} is 0.775 V, and corresponding minimal energy is $0.775^2 \times 15.9085 = 9.5550$ unit. Under this configuration, the delay by sizing the gate has reached minimum, so no V_{dd} lower than 0.775 V can reach a delay equal or lower than 1.5×minimal delay. So, the possible range of V_{dd} is $[0.775, 1]$. At the boundary of the range, which is 0.775 and 1, the minimal energies are achieved by adjusting only V_{dd} and gate size respectively, so the E_{min} would be larger than intermediate part. The prediction of the trend of the E_{min}~V_{dd} curve would be downward at first, and then upward.

3.3.2. Solving E_{min}~V_{dd} curve at 1.5×minimal delay. Since the range of V_{dd} is determined, it is possible to choose value in the range uniformly and calculate the E_{min} for the chosen V_{dd} respectively. The constraint equation is:

$$D = (\sum(g_i \cdot h_i \cdot b_i + p_i)) \cdot \frac{V_{dd}}{(V_{dd}-V_{th})^2} = 111.33 \pm 2 \tag{11}$$

There is a small range for the delay in case no solution due to finite step.

The solved result is in table 5 and corresponding graph is illustrated in figure 10.

Table 5. Relationship between V_{dd} and E_{min}

V_{dd} / V	E_{min} / Unit
0.775	9.555
0.795	6.312
0.815	5.916
0.835	5.926
0.855	6.018
0.875	6.188
0.895	6.369
0.915	6.595
0.935	6.829
0.955	7.070
0.975	7.323
0.995	7.627

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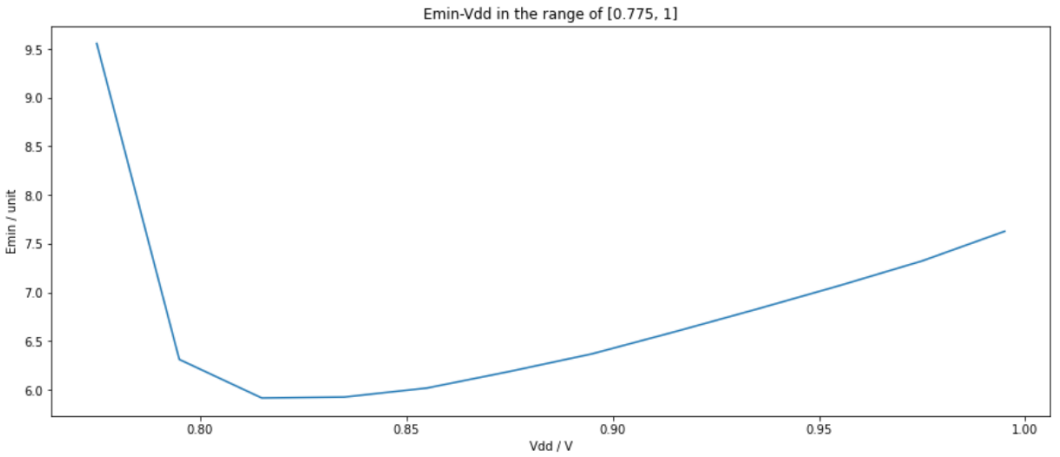

Figure 10. E_{min}~V_{dd} curve (Photo/Picture credit: Original)

The graph shows that the trend fits the previous prediction: the trend of the E_{min}~V_{dd} curve would be downward at first, and then upward. To get an overall minimal energy at 1.5×minimal delay, the best V_{dd} is 0.815 V. The comparation between: 1. Adjust V_{dd}only; 2. Adjust gate-size only; 3. Adjust both variables at the same time, is as follows in table 6.

Table 6. Methods and corresponding minimal energy

Method	E_{min} / Unit	Percentage of saved energy
Adjust V_{dd} only	9.555	39.9%
Adjust gate-size only	7.627	52.1%
Adjust both variables	5.916	62.8%

4. Conclusion and prospect

The research designed a 4-bit abs-value detector with low delay and reduce its energy consumption by sacrificing fifty percent of its processing speed. The MUX-based adder implementation of abs-value calculator would decrease the delay significantly for positive inputs. And a comparator from LSB to MSB would lower the general delay of the circuit. Implementing XOR and MUX with CMOS instead of compound gates would also save energy and processing time. Among all 3 ways of lowering energy consumption, adjusting both V_{dd} and gate-size has the greatest percentage of energy saving, which is 62.8%. For specific BMI circuit whose priority for speed requirements is lower than the energy efficiency requirements, the method of adjusting both V_{dd} and gate-size in this research would be significantly helpful.

The research has the following deficiencies: 1. The assumptions made in chapter 3.1 is not accurate enough. For example, in critical path, the MUX on the branch is actually the same MUX that in on the critical path. So, the assumption that all gates on the same stage have the same size as the corresponding gate on the critical path would be inaccurate. Meanwhile, it is possible to achieve a lower energy for the whole circuit by adjusting gate-size on non-critical path other than the same size as corresponding gates on critical path. 2. The algorithm used to calculate the minimal consumption for each V_{dd} is nearly brute force and has a very high complexity. Therefore, the range and step of each gate is limited on the critical path. And a smaller minimal energy with higher accuracy is possible.

The future study may improve the deficiencies mentioned for this research. It is meaningful to build a more precise relationship between energy consumption and each gate-size, instead of only focusing on critical path. And it is more efficient to optimize the algorithm with methods like binary search. This would make smaller step and wider range for each gate-size, and lead to a lower possible energy consumption. Besides, all the gates are implemented with CMOS style, but the gates are also

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possible to be achieved with Pass Transistor Logic (PTL) style. So further research can focus on the delay and energy consumption differences between CMOS and PTL.

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