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Novel five-level inverter based on DC power-capacitor series charge-discharge switching strategy

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Abstract. Photovoltaic power generation systems generally include four modules: solar cells, batteries, inverters and controllers. Among them, the inverter converts the direct current generated by the photovoltaic array into a power conversion device that meets the grid-connected requirements for industrial frequency alternating current, which is the key equipment for grid-connected photovoltaic power generation system. Most multilevel inverters in the market today are based on the Neutral-Point-Clamped (NPC) structure to generate voltages at different levels, and then control the magnitude and direction of the voltages through H-bridge circuits. This topology has been maturely used in three-level inverters, but if we want to build five-level, seven-level and more level numbers of inverters based on NPC, the number of capacitors used is increasing, and the circuit becomes more and more complex. Therefore, this paper proposes a five-level inverter topology based on single power supply-single capacitor series charging and discharging. (Power-capacitor series charge-discharge switching, PCSCDS). This inverter has a simple structure, comprehensible control strategy and requires only one DC power supply and one large capacitor to generate a five-level voltage. The topology is subsequently simulated and analyzed by MATLAB/Simulink simulation, which proves the effectiveness of the novel inverter.

Keywords: Novel topology, multilevel inverter, capacitor charge-discharge switching strategy, symmetrical structure.

1. Introduction

In recent years, with the large increase in fossil energy consumption represented by coal, oil and natural gas, the problem of worldwide energy crisis has become increasingly serious. Nowadays, almost every country in the world is vigorously developing various new energy technologies. China's current main development and utilisation of new energy are solar energy, wind energy, hydro energy, biomass energy, geothermal energy, hydrogen energy [1]. Among them, solar energy is infinite in reserves and free of pollutants. Moreover, it is of high utilization efficiency and with a short construction cycle [2]. Geographically, China's vast territory makes her being richer in solar energy resources, comparing with her Asian neighbouring countries at the same latitude [3]. Solar photovoltaic power generation is a popular method to extract solar energy, which has the advantage of stable power supply. Grid-connected, photovoltaic power generation system can rely on the public power grid to deliver stable power resources to the community [4]. Under the tendency of global development of photovoltaic power generation, China's photovoltaic industry is also developing rapidly. Photovoltaic power generation

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systems generally include four modules: solar cells, batteries, inverters and controllers, as shown in Figure 1. Among them, the inverter converts the direct current generated by the photovoltaic array into a power conversion device that meets the grid-connected requirements for industrial frequency alternating current, which is the key equipment for grid-connected photovoltaic power generation system.

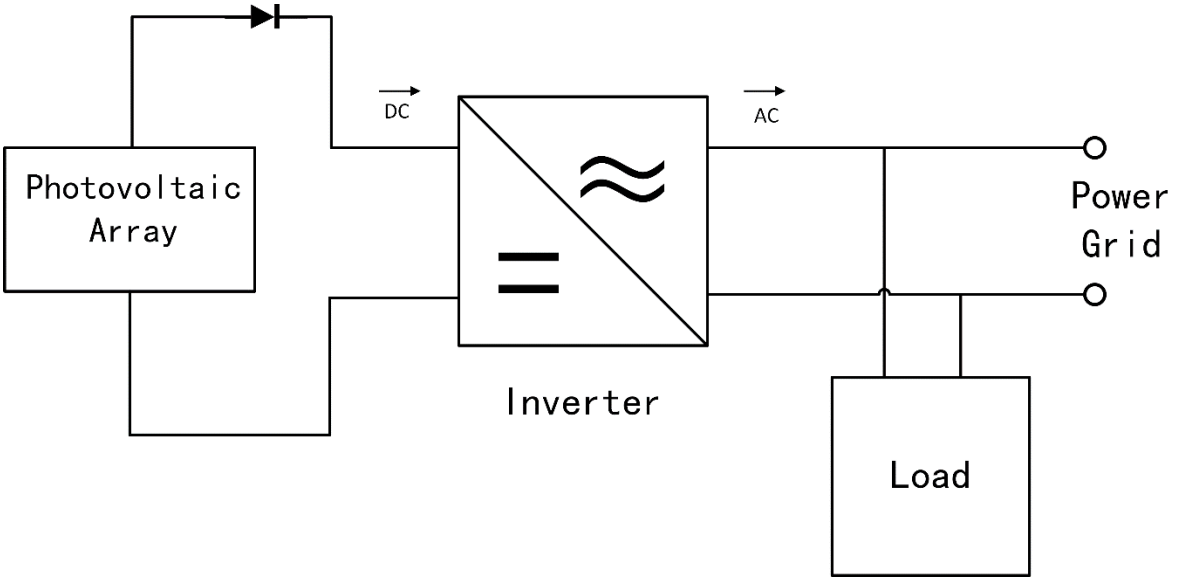

Figure 1. Photovoltaic power generation system structure [4].

Conventional two-level half-bridge inverter require only two power devices, which is economical, simple, and have a comprehensible control strategy while eliminates leakage currents. However, the output DC voltage of the power generation system needs to be twice the peak voltage of the grid, and the switching devices need to withstand the voltage stress of the entire DC bus [5], which not only affects the lifespan of the switching devices, but also restricts the development of the inverter towards higher voltages. In order to reduce the switching device stress and filter size, multilevel inverter topology can be adopted. Multilevel inverters are gradually emerging by virtue of their high voltage tolerance and better voltage waveforms which is closer to sinusoidal waveforms.

Currently, the widely used multilevel inverter topologies in photovoltaic mainly include diode Neutral-Point-Clamped structure (NPC), Flying-Capacitor structure (FC), and Cascade H-Bridge structure (CHB). Among them, the NPC inverter's circuit is relatively simple, the control strategy is easy to implement. But there is a fundamental problem of uneven voltage division by DC capacitors. Worldwide research is still underway on how to achieve the mid-point voltage balance of the NPC inverter [6].

FC inverter improves the problem of voltage imbalance of the NPC inverter, but it requires a large number of clamping capacitors, which leads to the huge size of the overall circuit and a complex control strategy [7]. When constructing inverters with five or even seven levels or more, the number of DC power supplies and switching tubes required by CHB inverters increases rapidly, and the economic cost is relatively high. In recent years, many scholars have proposed new topologies for constructing five-level inverters. Literature [8] proposes a split symmetrical five level inverter with a split structure which requires only one power supply to output five levels and improves the drawbacks of capacitor voltage imbalance in NPC inverters, but the number of capacitors used in this topology is high. Literature [9] uses a symmetrical structure of two independent power sources to supply power directly, avoiding the problems of too much capacitance and capacitor voltage imbalance. but the structure requires two DC power sources, the application conditions are slightly more demanding. Literature [10] proposes the structure of supplying power through one unit of DC source and another unit of capacitor power supply,

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which provides an effective solution to the above problem, but the control principle is more complicated and a voltage regulator control needs to be introduced to stabilise the capacitor voltage in the control strategy.

In order to overcome the above drawbacks, this paper proposes a power-capacitor series charge-discharge switching (PCSCDS) five-level inverter topology, which requires only a single DC power supply and a single capacitor to output a five-level waveform. The single capacitor in this topology is directly supplied by the DC power supply. Thus, the structure does not produce the capacitor imbalance problem generated in the NPC inverters; moreover, the control strategy adopted in this inverter makes the capacitor discharge in only two modes during one operating cycle, the capacitor charging time is longer than the discharging time, making the capacitor have the enough electric quantity when discharging.

2. Topological and modal analysis

The topology is shown in figure 2. It uses 1 DC voltage source, 1 capacitor, 1 resistor, 6 IGBT switches with reverse fast diodes and 2 IGBT switches without reverse fast diodes. In this topology, by controlling the switching tube, the DC source can be connected in series with the capacitor in some modes, charging the capacitor in reverse and provide the load with a single DC voltage. In the other modes, the DC source and the capacitor are connected in series in the same direction. The capacitor discharges and together with the DC source to provide the load with twice the DC voltage.

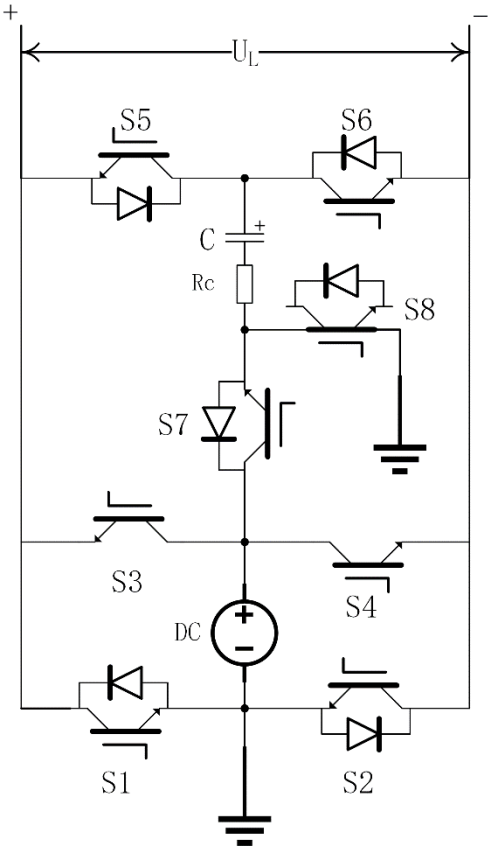

Figure 2. Power-capacitor series charge-discharge switching Five-Level Inverter topology (Photo credit: Original)

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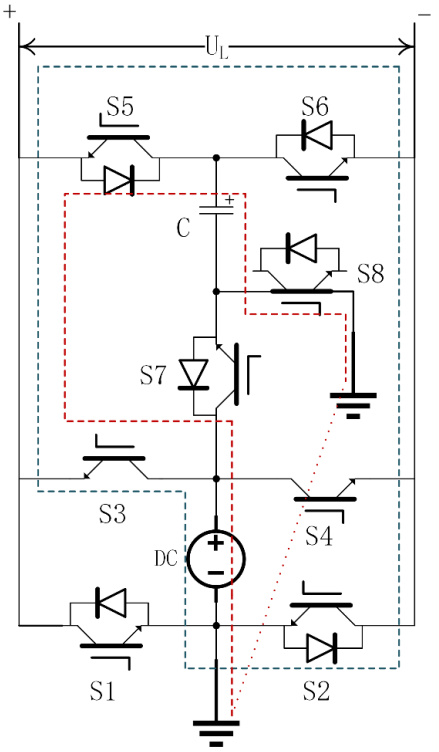

Figure 3. Mode 2 (Photo credit: Original)

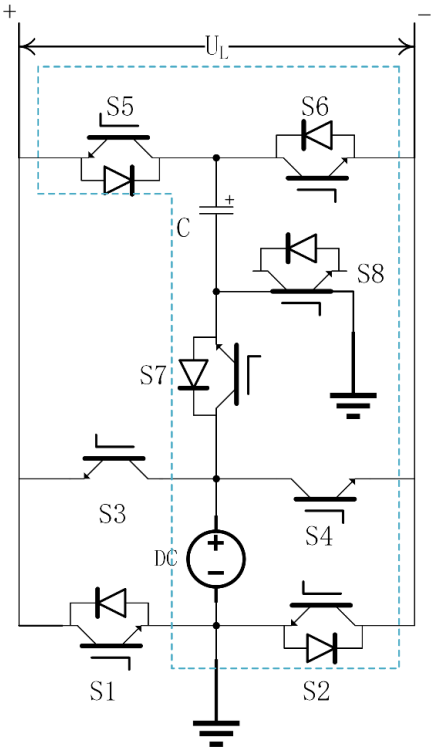

Figure 4. Mode 3 (Photo credit: Original)

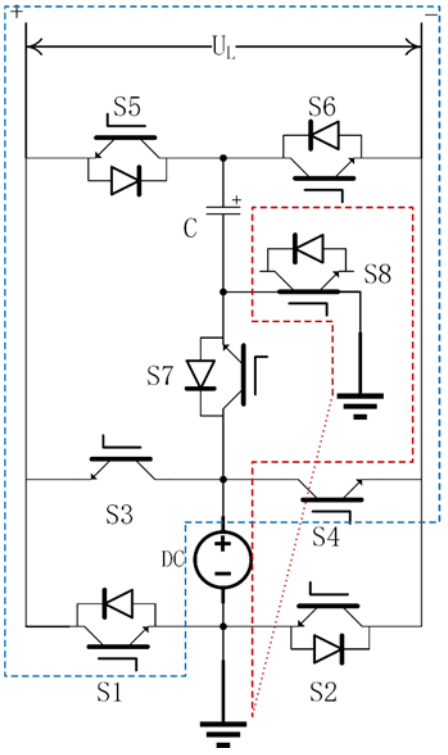

Figure 5. Mode 4 (Photo credit: Original)

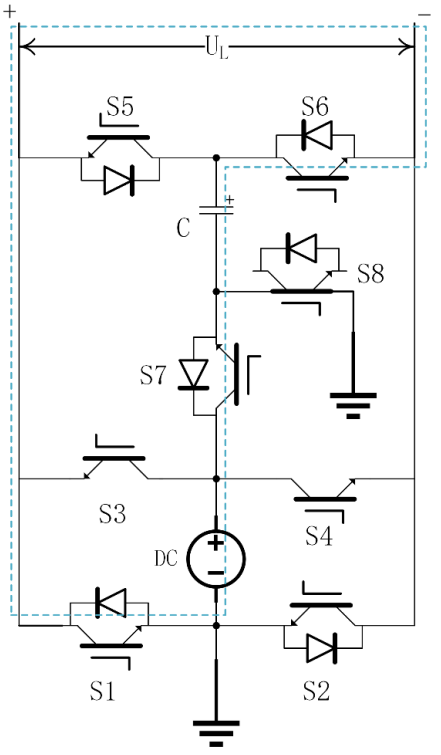

Figure 6. Mode 5 (Photo credit: Original)

Mode 1: Figure is abbreviated, S1-S7 are off, S8 is on, there is no loop in the circuit at this point. $U_L = 0$

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Mode 2: As shown in Figure 3, S1, S4, S5, S6, S7 are switched off; S2, S3, S5, S8 conduct. In this case the load is supplied directly from the DC power supply. Capacitor is charging. U_L=V_{in}. Voltage stress: V_{s1}=V_{s4}=V_{s6}=V_{s7}=V_C=V_{in}

Mode 3: As shown in figure 4, S1, S3, S4, S6, S8 are switched off; S2, S5, S7 conduct. In this case the load voltage is provided by the DC power supply and capacitor together in series. Capacitor is discharging. U_L= $2V_{in}$ Voltage stress: V_{s3}=V_{s4}=V_{s8}=V_C=V_{in}; V_{s1}=V_{s6}=$2V_{in}$

Mode 4: As shown in figure 5, S2, S3, S5, S6, S7 are switched off, S1, S4, S8 conduct. In this case the load is supplied directly from the power supply. Capacitor is charging. U_L= $-V_{in}$ Voltage stress: V_{s2}=V_{s3}=V_{s5}=V_{s6}=V_{s7}=V_C

Mode 5: As shown in figure 6, S2, S3, S4, S5, S8 are switched off; S1, S6, S7 conduct. In this case the load voltage is provided by the DC power supply and capacitor together in series. Capacitor is discharging. U_L= $-2V_{in}$ Voltage stress: V_{s3}=V_{s4}=V_{s8}=V_C=V_{in}; V_{s2}=V_{s5}=$2V_{in}$

3. Modulation method

3.1. Modulated wave analysis

In this paper, phase disposition PWM technique is used for modulation. Four triangular carriers of the same amplitude and frequency are superimposed and compared with the sinusoidal modulated wave, as shown in Figure 7.

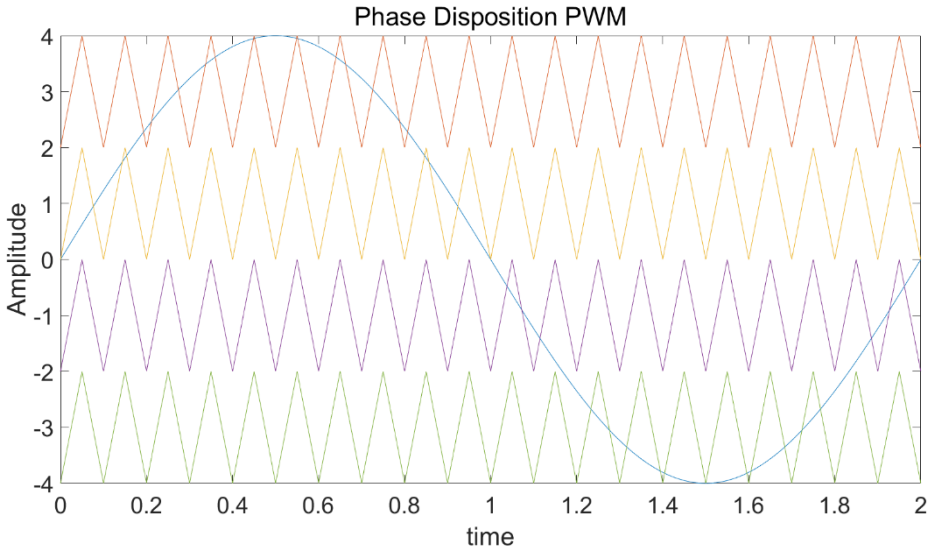

Figure 7. Phase disposition PWM (Photo credit: Original)

3.2. Control strategy analysis

Figures 8 to 11 showed the waveform of e1~e8, which are the conduction signals of S1-S8, respectively.

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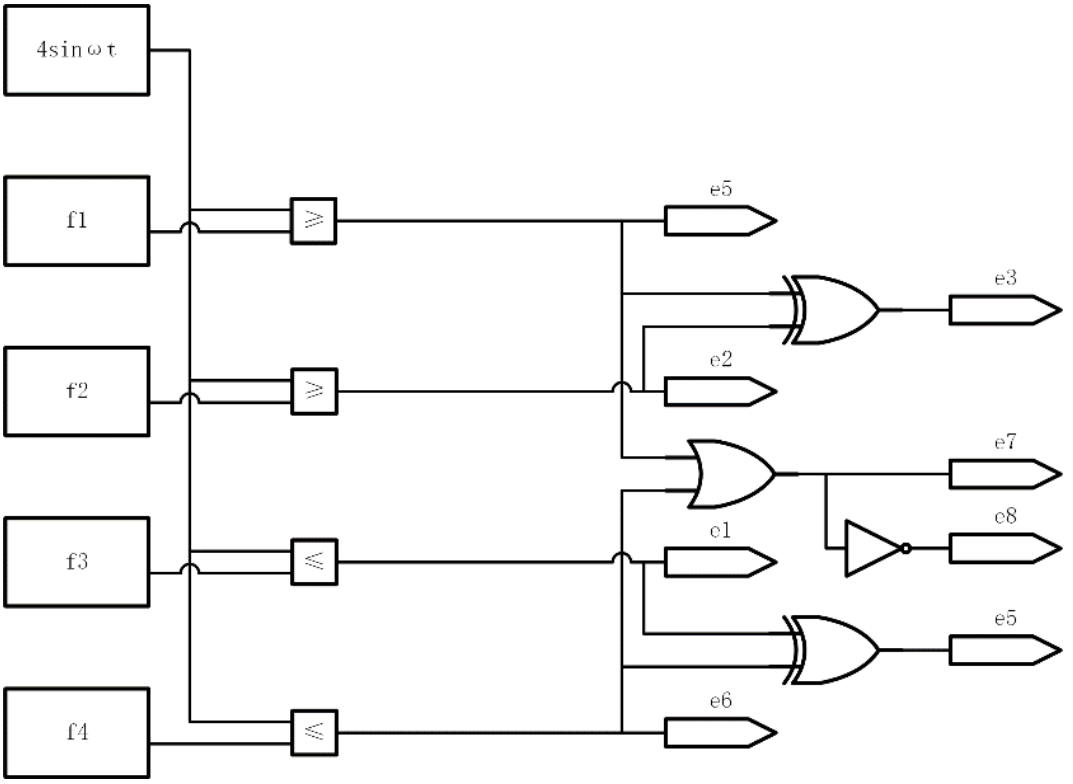

Figure 8. Control strategy logic diagram (Photo credit: Original)

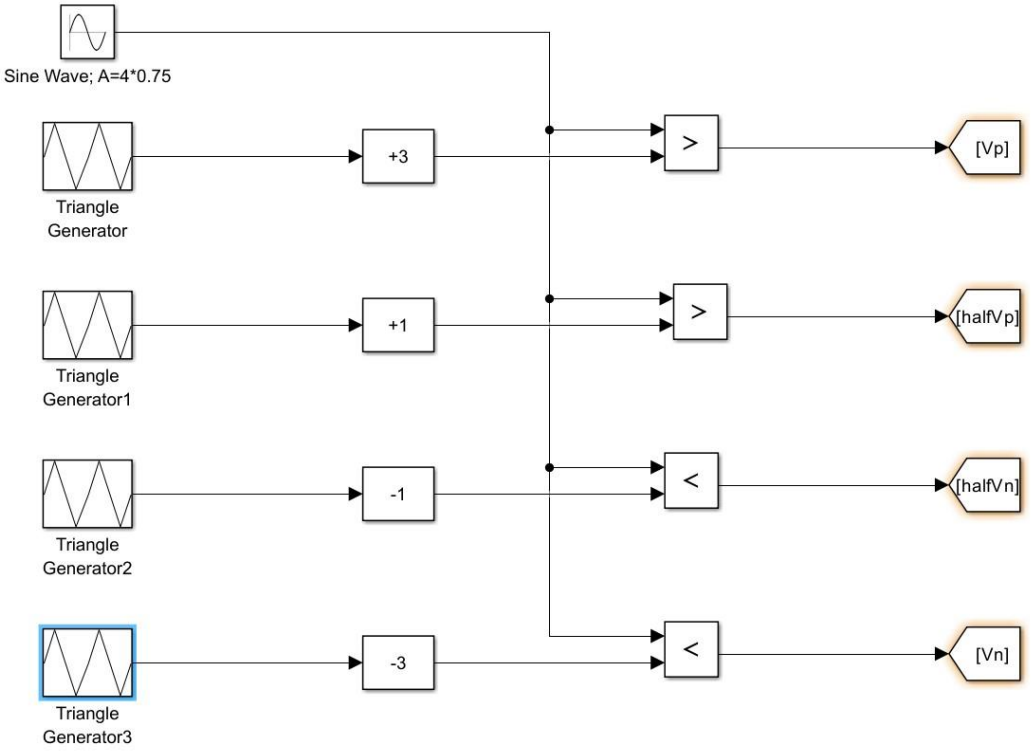

Figure 9. Control circuit built in the simulation (Photo credit: Original)

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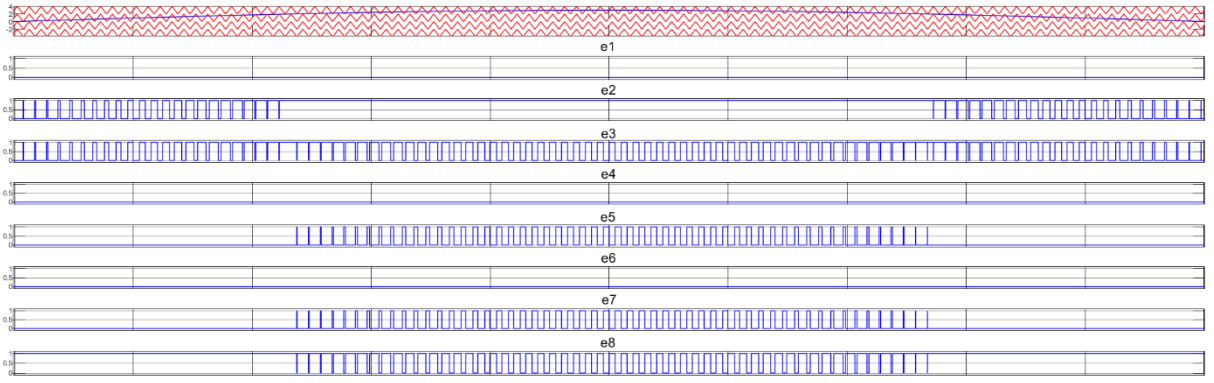

Figure 10. Signal variation of e1-e8 (first half cycle) (Photo credit: Original)

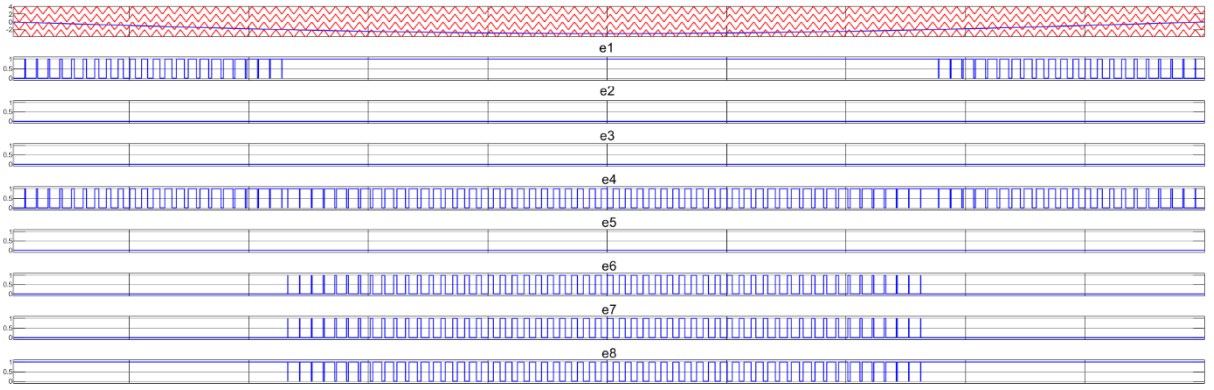

Figure 11. Signal variation of e1-e8 (second half cycle) (Photo credit: Original)

4. Parameter design and simulation

4.1. Design of current limiting resistor

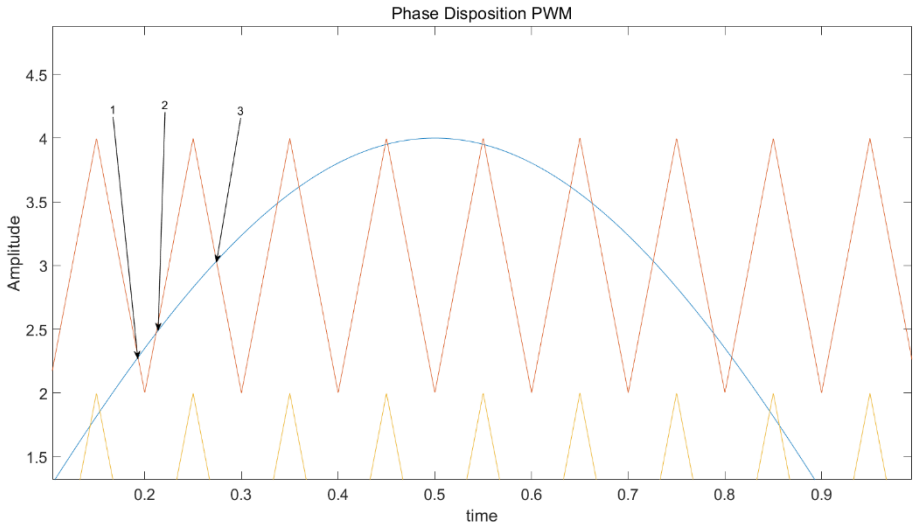

Figure 12. Division of the carrier wave (Photo credit: Original)

Set A_m be the modulating wave amplitude, A_{er} be the carrier wave amplitude, then:

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$$m_a = \frac{A_m}{4A_{er}} \tag{1}$$

The expression of sinusoidal modulated waveform V_m is:

$$V_m = 4m_a \sin \omega t \tag{2}$$

Divide the highest carrier wave into 3 straight line sections as the figure shown.
Set T_{er} be the carrier period. Then the linear equations of carrier segments 1, 2, 3 are:

$$\begin{cases} v_1 = -\frac{4}{T_{er}} t + 10 \\ v_2 = \frac{4}{T_{er}} t - 6 \\ v_3 = -\frac{4}{T_{er}} t + 14 \end{cases} \tag{3}$$

At t_1,t_2 moments, the following equation is satisfied:

$$\begin{cases} 2m_a \sin \omega t = -\frac{2}{T_{er}} t + 5 \\ 2m_a \sin \omega t = \frac{2}{T_{er}} t + 3 \end{cases} \tag{4}$$

Then the duty cycle of the sine wave over the triangular wave portion can be found to be:

$$\tau_1 = \frac{t_2 - t_1}{T_{er}} = 2m_a \sin\ \omega t - 1 \tag{5}$$

From the control strategy in this paper, it can be obtained that τ_1 Part of the capacitor discharges.
The voltage after a discharge period:

$$V_C = V_0 e^{-\frac{t}{C*R_L}} \tag{6}$$

Set i_C be the capacitor current, then:

$$i_{Cmax} = \frac{V_0 - V_C}{R_c} \tag{7}$$

i.e.

$$R_c = \frac{V_0(1+\ln(\frac{C*R_L}{-t}))}{i_{Cmax}} \tag{8}$$

4.2. Design of capacitor parameters

In mode 2 and mode 4 the load is powered in series by DC power source and the capacitor together, so the capacitor will inevitably have some degree of ripple voltage drop when discharging. Introduce ripple voltage drop amplitude

$$\mu\% = \frac{V_0 - V_C}{V_0} \tag{9}$$

In this paper, it is argued that if the maximum voltage drop does not exceed 1%, The outcome voltage waveform can be obtained as a one with high quality. The fluctuation of capacitor voltage is analysed as follows. Neglecting the load inductive reactance. Set the load resistance be R. The instantaneous value of the capacitor voltage during discharge is:

$$V_C = V_0 e^{-\frac{t}{C*R_L}} \tag{10}$$

To wit:

$$C = \frac{t}{R_L * \ln \frac{V_0}{V_C}} \tag{11}$$

Bringing the voltage drop magnitude into the equation gives:

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$$C = \frac{t}{R_L * \ln\left(\frac{1}{1-\mu\%}\right)} \tag{12}$$

included among these:

$$t = \tau_1 T_{er} \tag{13}$$

Table 1. Case Parameters

	f_{er}	f_m	R_L	V_{in}	C	m_a	R_c
Case 1	10kHz	50Hz	100Ω	400V	50μF	0.75	0Ω
Case 2	10kHz	50Hz	100Ω	400V	50μF	0.75	0.25Ω
Case 3	10kHz	50Hz	100Ω	400V	10μF	0.75	0.25Ω

4.3. Simulation analysis and topological improvements

The simulation is carried out on the MATLAB/Simulink tool. Table 1 summarized the case parameter.

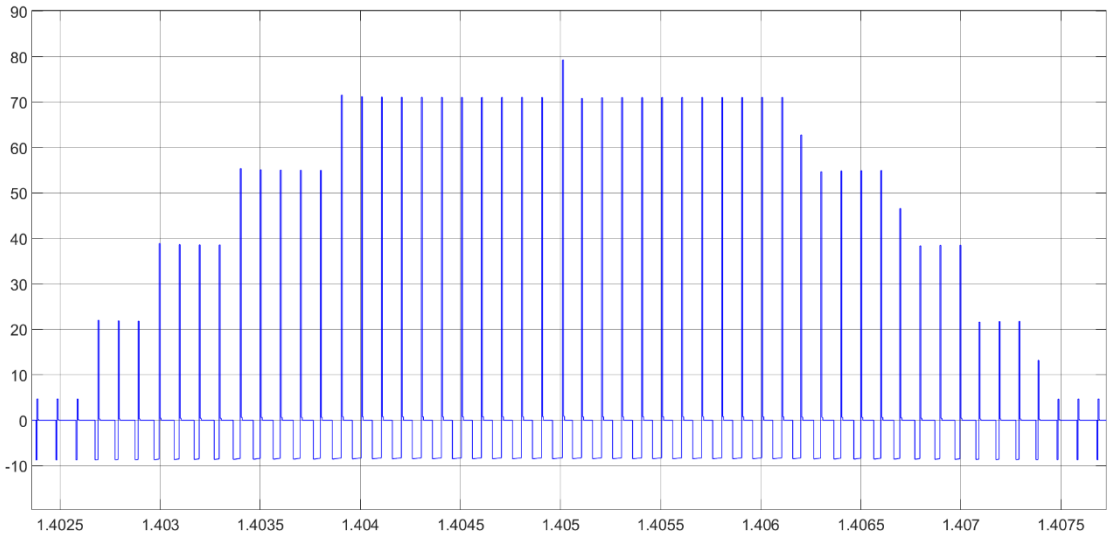

Figure 13. Capacitor current i_C in case1 (Photo credit: Original)

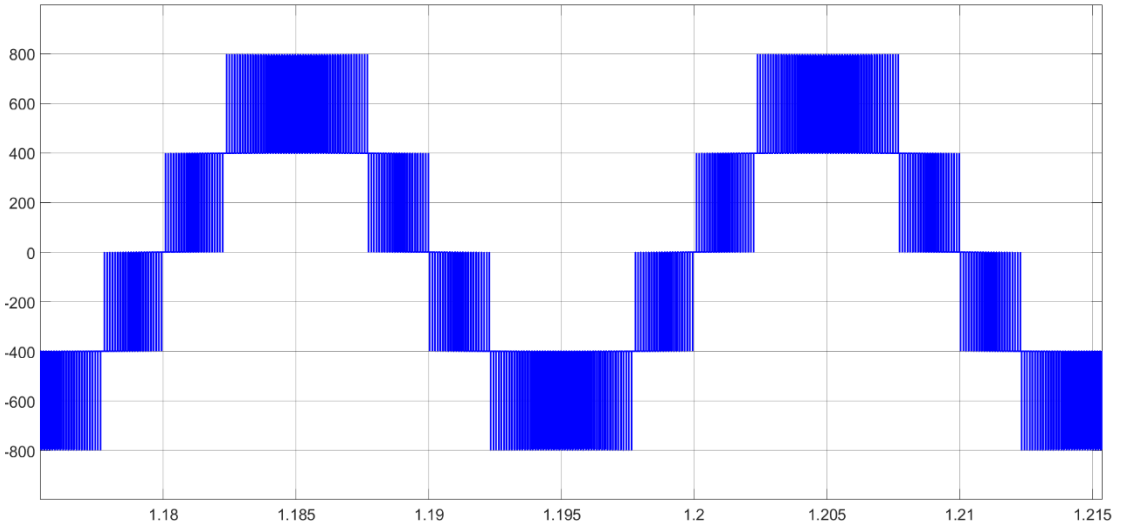

Figure 14. Load voltage U_L in case1 (Photo credit: Original)

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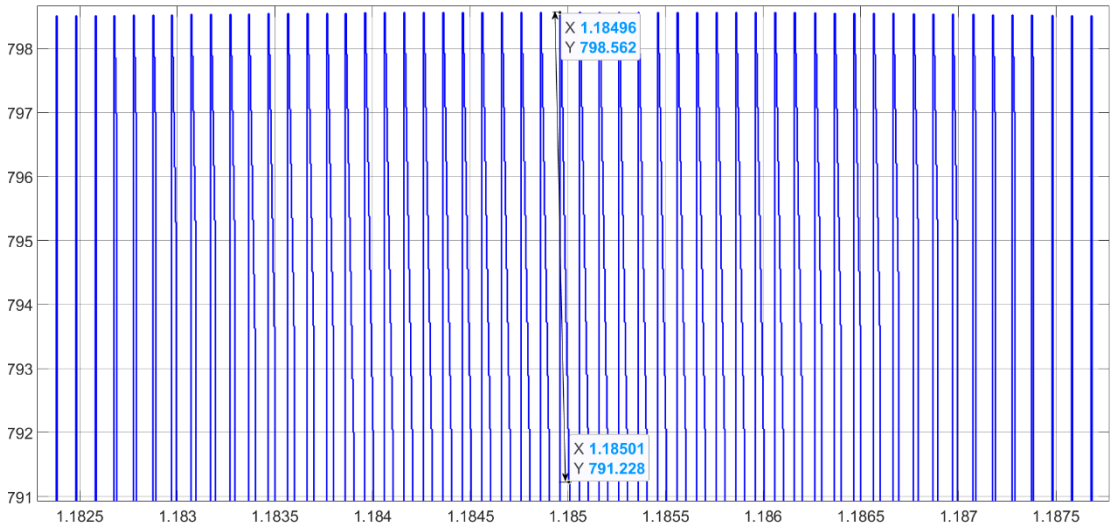

Figure 15. Capacitor ripple voltage drop in case1 (Photo credit: Original)

The result of case 1 are shown in Figures 13 to 15. As the pattern shows ΔV=7.334V. To wit $\mu\%$ =0.917%<1%, $\mu\%$ <1% means the outcome wave is of high quality, justifies the topology. Nevertheless, the current output of the capacitor is way too high, which is likely to result in a circuitry burnout. Therefore, a current limiting resistance should be applied.

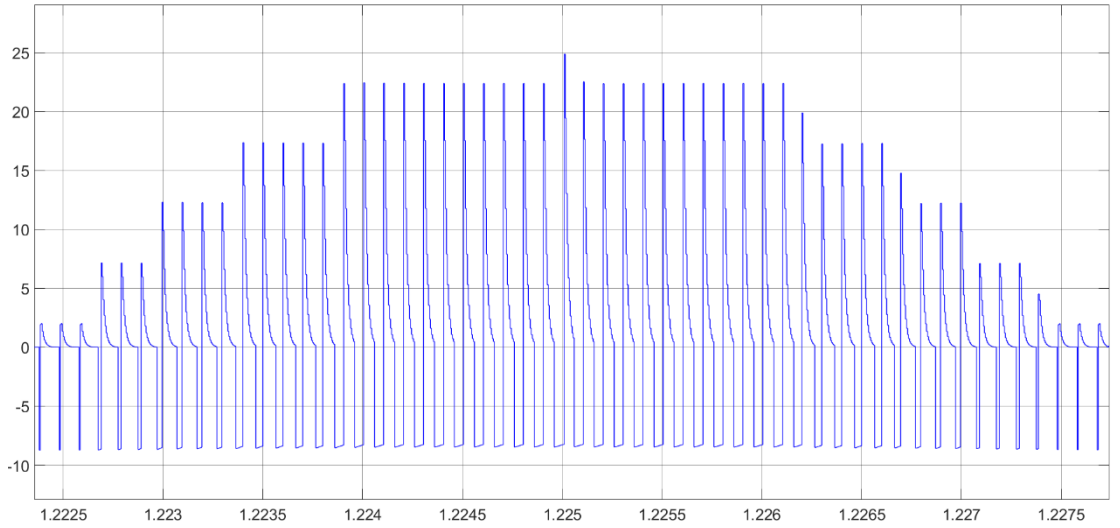

Figure 16. Capacitor current i_C in case2 (Photo credit: Original)

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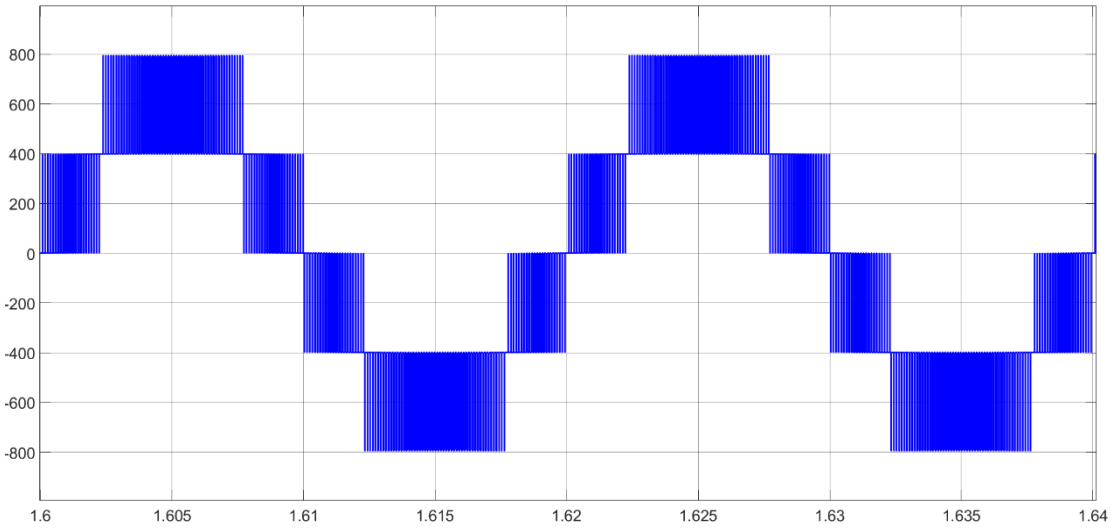

Figure 17. Load voltage U_L in case2 (Photo credit: Original)

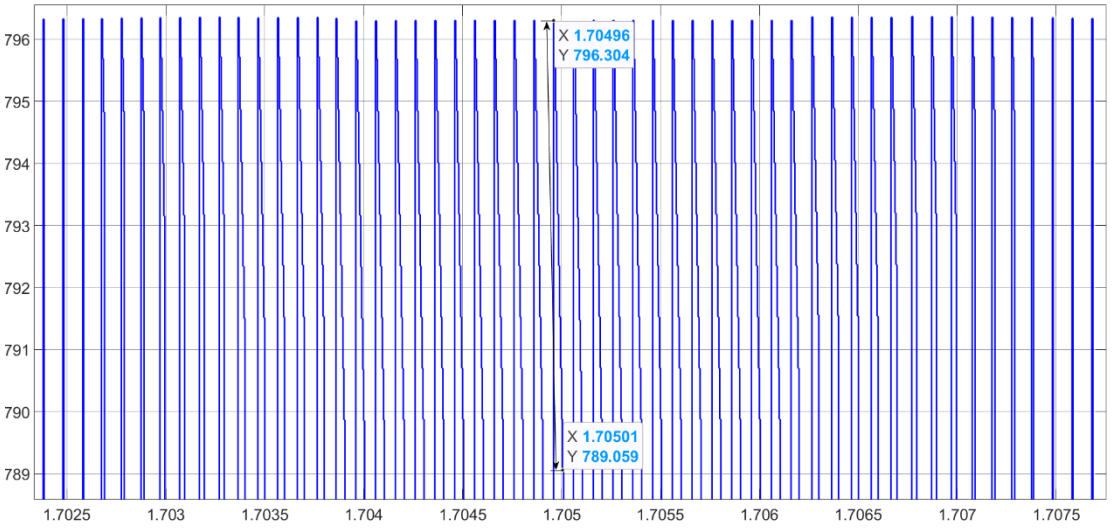

Figure 18. Capacitor ripple voltage drop in case2 (Photo credit: Original)

In case 2, as shown in Figure 16 and 17, the circuit is more secure with the current limiting resistor, which should be adjusted to different situations. As figure 18 shows ΔV=7.245V. The outcome voltage waveform is still of high quality.

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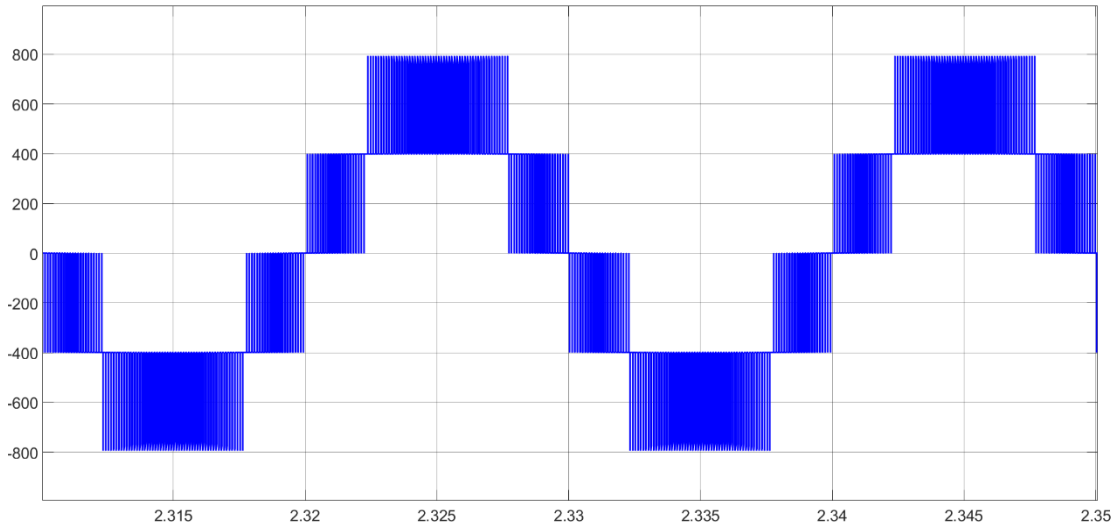

Figure 19. Load voltage U_L in case3 (Photo credit: Original)

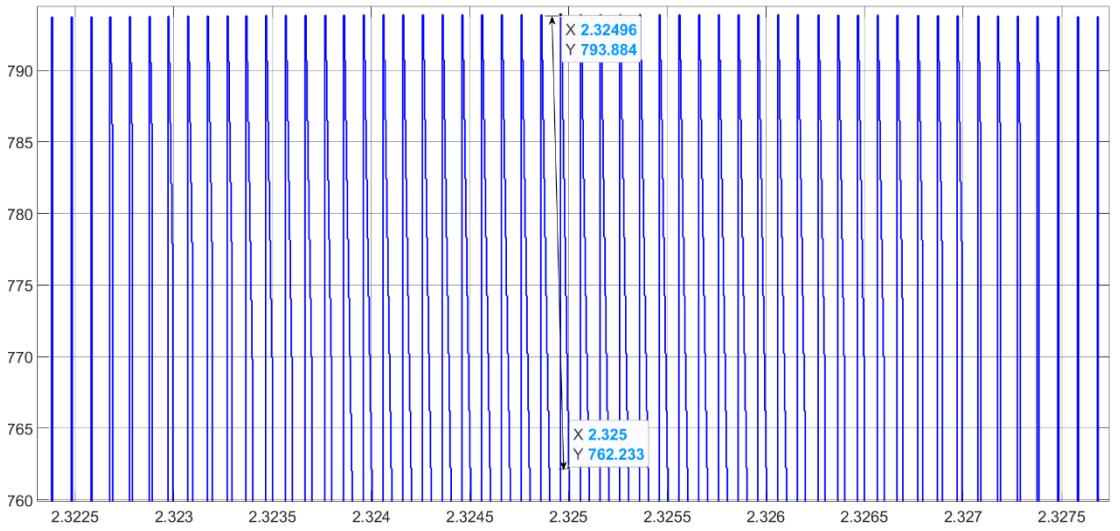

Figure 20. Capacitor ripple voltage drop in case3 (Photo credit: Original)

Figure 19 and 20 showed the results of case 3, where ΔV=31.651V; μ%=3.956%. As shown in figure 20, the magnitude of the ripple voltage drop massively increases when the capacitance is reduced.

5. Conclusion

In this paper, a novel five-level inverter based on DC power-capacitor series charge-discharge switching strategy is proposed. By analysing its topology and circuit simulation, the following conclusions are drawn. Firstly, the topology of this paper is a single power supply-single capacitor structure, which does not require multiple power supplies or multiple capacitors. Moreover, the number of components used is less compared to other five-level inverters, which is economical and effective. The structure and the control strategy are simple and easy to understand as well. Secondly, by analysing the relationship between the ripple voltage drop magnitude μ%, capacitance C and load equivalent resistance R, this paper derive Equation, which provides a reference for choosing a suitable capacitor to design a standard-compliant inverter. The subsequent simulation also proves the correctness of the equation.

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References

[1] ZHANG J, XI J, HU J. Research review of new energy technologies [J]. *Shandong Chemical Industry*, 2018, 47(19): 75, 83.

[2] XU Z. Analysis of the application advantages of solar photovoltaic power generation system in civil buildings[J]. *Lamps & Lighting*, 2022,5(167): p119-121.

[3] ZHANG X. Research on grid-connected voltage stability and voltage regulation strategy of photovoltaic power generation [D]. Changchun: *Jilin University of Architecture*, 2023

[4] LIU X. Research on solar photovoltaic power generation and related technologies[J]. *China Equipment Engineering*, 2023(9): p207-209.

[5] ZHU X. Research on topology and control technology of single-phase multilevel photovoltaic grid-connected inverter [D]. Changsha: *Hunan University*, 2022.

[6] YU, T. Research on optimal modulation strategy of midpoint clamped three-level inverter [D]. Wuhan: *Huazhong University of Science and Technology*, 2022.

[7] CHENG C, HE L. Flying-capacitor-clamped five-level inverter based on switched-capacitor topology [C] / / *2016 IEEE Energy Conversion Congress and Exposition (ECCE 2016)*, September 18 - 22, 2016, Milwaukee, WI, USA. 2016: 1 -

[8] ZHANG S, LIU Y, DU X, HUANG Z, JIA Y, WANG P, ZHANG J. A differential symmetrical five-level inverter topology and analysis[J]. *Electrical Machines and Control Applications*, 2023,50(8): p52-59.

[9] YE M, LIU W, YU S, XING R. Novel eight-switch five-level inverter and power balanced modulation strategy[J]. Journal of Electrical Machines and Control, 2023,27(5): p138-148

[10] YANG Z, TANG H. Research on the regulation strategy of single-supply type five-level inverter[J]. *Journal of Solar Energy*, 2021,42(12): p452-458.