

Research and Characteristic Analysis of MOSFET Short Channel Effect Based on Simulation

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Abstract: This study focuses on the short-channel effect of metal-oxide-semiconductor field-effect transistors (MOSFETs). It begins by outlining the development history of MOS transistors, which, as the cornerstone of integrated circuit technology, have undergone a long process from concept to technological maturity. With the advancement of integrated circuit manufacturing processes, the channel length of MOSFETs has been reduced to the nanometer scale, leading to the emergence of the short-channel effect. The paper then delves into the principles of the short-channel effect, including mechanisms such as threshold voltage reduction, increased drain current, and decreased transconductance. Experiments were conducted by designing NMOS transistors with different channel lengths (100nm - 500nm), and transfer characteristic curves were plotted and analyzed. Additionally, Sentaurus software was used to simulate the electrical characteristics of MOSFETs with different channel lengths: transfer characteristics, potential distribution, and electric field distribution. The results show that long-channel devices have strong carrier control ability, high threshold voltage, low power consumption, and good stability; short-channel devices exhibit reduced threshold voltage, increased drain current, intensified channel length modulation effect, and degraded switching performance. The research conclusions provide theoretical and data support for addressing the short-channel effect in integrated circuit design.

Keywords: MOSFET, Short-Channel Effects, Transconductance, Channel Length Modulation, Integrated Circuit Design

1. Introduction

1.1. MOSFET technology evolution

The MOSFET, or Metal-Oxide-Semiconductor Field-Effect Transistor, is an indispensable basic component in modern electronics and a cornerstone of integrated circuit technology [1]. The concept of the field-effect transistor was first proposed by American physicist Julius Edgar Lilienfeld in the 1930s [2]. The MOS technology was finally introduced by Shockley and his team at Bell Labs in 1959, marking the birth of the MOS transistor. The practical application of MOS technology in integrated circuits by Motorola signified the completion of the practical process of MOSFET technology [3].

1.2. Short-channel effects

In the late 1970s, with the wide application of integrated circuits, their manufacturing processes were constantly improving, and people's demands for the size of these semiconductor devices were getting smaller and smaller [4]. As a result, the channel length of MOSFETs decreased from the original micrometer level to the nanometer level and even smaller. However, as the channel length shrank, the devices exhibited behaviors that did not conform to traditional physical models [5]. This is often classified as secondary effects of small-sized devices in the design of integrated circuits. Among them, the impact on the control ability of the gate voltage over MOS devices is the most significant: a significant decrease in threshold voltage and an increase in drain current [6].

2. MOS device design and short-channel effect principles

2.1. Principle of short channel effect

The basic principle of short channel effect is that with the reduction of device size, the channel length of MOSFET shrinks, making the gate length (that is, source and drain) further shorter [7]. Because the source and drain form PN junction for the substrate, there is a space charge region between P-type doping and N-type doping, forming a threshold voltage formula when the channel length changes short:

$$V_T = V_{FB} + 2\phi_{FB} - \frac{Q_A}{C_{OX}} \quad \text{and} \quad Q_A = -qN_A X_d = -(4\epsilon_s q N_A \phi_{FB})^{\frac{1}{2}} \quad (1)$$

Here, Q_A is the charge accumulated in the depletion region under the channel (the charge from the gate voltage). At this time, the built-in potential of the source drain and substrate PN junction on both sides will also provide charge to the side near the channel, resulting in a decrease in the proportion of charge provided by the gate under the gate oxide layer. Therefore, the average charge density under the gate oxide layer decreases, resulting in a decrease in Q_A , and finally a decrease in the threshold voltage [8]. At the same time, with the shortening of the channel length, the same source-drain voltage will produce a greater electric field strength in the horizontal, because the charge velocity is related to the electric field strength:

$$v = \begin{cases} \frac{\mu_0}{1 + \frac{V_{GS} - V_T}{V_K}} E_y, & E_y < E_c \\ v_{max} = C, & E_y \geq E_c \end{cases} \quad (2)$$

The increase of the electric field intensity will lead to velocity saturation, so the drain current will also reach saturation when the carrier concentration is constant (doping is certain).

In addition, from the perspective of the transconductance of the device, the short channel length of the MOS device often leads to a larger source leakage field, resulting in a larger source and drain voltage V_{DS} , so that its influence on the drain current is intensified. Due to the transconductance of MOS transistors $g_m = \frac{\delta I_D}{\delta V_{GS}}$, one of the important indicators of transistor performance, its size is related to the MOSFET's adjustment ability under different gate source voltages. Under ideal conditions, transconductance g_m is positively correlated with current. When the channel becomes shorter, the leakage current is affected by the source-leakage voltage, and the change of the leakage current caused by the grid voltage regulation decreases, so that the transconductance decreases.

2.2. MOS design of different channels and introduction of ID transfer characteristic curve

In the experiment, MOSFETs with different channel lengths were designed, and only NMOS was used as the experimental object for convenience, which is shown in Fig. 1. At the same time, in order to show the influence of channel effect more clearly, only two sides of the source and drain region, gate polysilicon and channel are retained in the device structure design. Phosphorus with a concentration of $1 \times 10^{20} \text{ cm}^{-3}$ is added to the source and drain of the MOSFET, and $1 \times 10^{17} \text{ cm}^{-3}$ boron is added to the channel. The channel length is given different parameters: 100, 150, 200, 250, 300, 500 (nm). In the figure, the sky blue part is the gate silica, the red part is the phosphorus-doped source and drain, and the dark blue part is the channel.

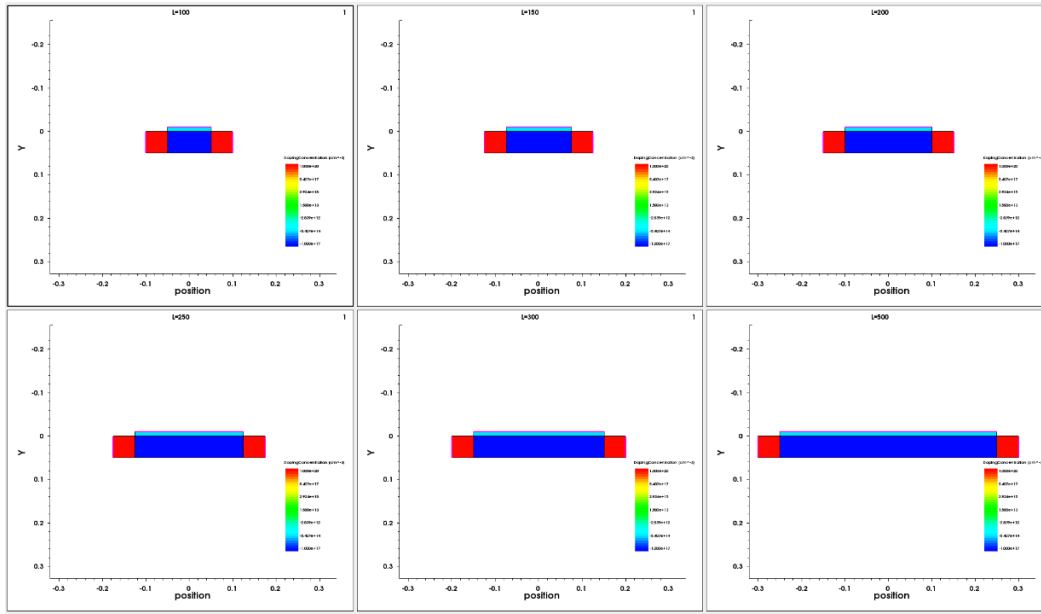


Figure 1: MOSFETs with different channel lengths

Transfer characteristic curve: Transfer characteristic curve is based on the fixed source and drain voltage (V_{DS}) to show the relationship between the saturation leakage current and the gate source voltage. This relationship is an important performance index to explain the control of V_{GS} to I_d and the reaction of MOS devices [9]. By drawing the transfer characteristic curve, the switching status and threshold voltage of the MOSFET can be understood. In this, the threshold voltage (V_{th}) refers to the minimum gate source voltage opened by the MOS tube, when the gate voltage (V_{GS}) is less than the threshold voltage, the MOSFET is in the subthreshold region, at this time the drain current is very small, the MOS tube is in the off state, although from a macro point of view, the drain current is very small, it actually still has an exponential function relationship [10]. As the grid voltage continues to increase, the drain current gradually increases, and the two show a linear relationship:

$$I_D = K(V_{GS} - V_{th})V_{DS} \quad (3)$$

When the MOSFET enters the saturation region, the saturation region current follows the formula:

$$I_D = \frac{1}{2} K (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (4)$$

Among them, V_{DS} is the drain-source voltage, and this term reflects the extent to which the drain current is affected by the drain-source voltage. At this point, the drain current no longer shows significant changes with the variation of the gate voltage, and a saturation phenomenon occurs. The

Fig. 2 shows the changes in the drain current under different gate voltages. From the result graph, it can be seen that when the gate voltage is relatively small, the drain current first increases exponentially, then shows a linear trend, and after exceeding the critical value, the growth rate gradually decreases.

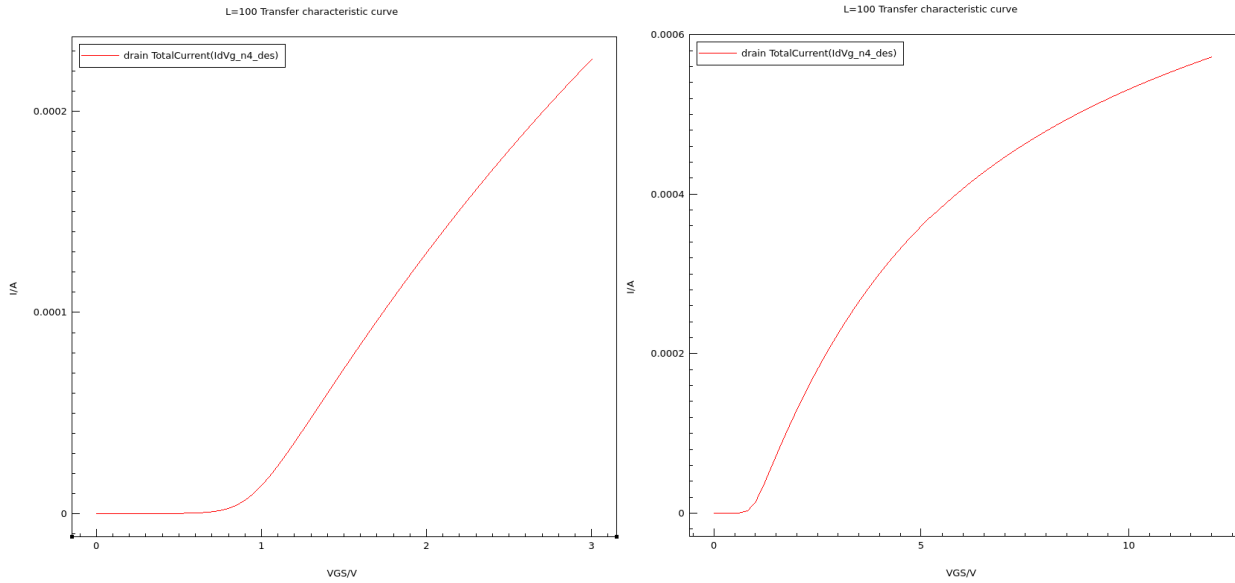


Figure 2: Transfer characteristic curve of the changes in the drain current under different gate voltages

3. MOS simulation and characteristic analysis with different channel lengths

3.1. Simulation of I_d transfer characteristics

This experimental simulation is based on the modeling and simulation design of Sentaurus software, and subsequent simulation is carried out on the established model. The simulation results are shown in Fig.3. The transfer characteristic curve is drawn by adjusting the input voltage V_{GS} of the grid and measuring the total drain current. In the experiment, there are 6 channels of different lengths, which are 100nm, 150nm, 200nm, 250nm, 300nm and 500nm respectively.

In the long channel, the transfer characteristic curve presents obvious linear relationship and small slope. This shows that the drain current varies less when the gate voltage changes, so the channel electric field of the long-channel MOS device has a strong ability to control the charge carriers. In addition, because the drain current is relatively small, long-channel devices perform better as low-power devices. At the same time, it is not difficult to find that the threshold voltage of the long channel device is larger, and the long channel device is not easy to open under the same voltage. Therefore, long-channel devices have a larger "switch" region. In practical applications, such devices have better voltage performance and stability, whether they are used in low-power circuits or high-voltage circuits, they can play a good electrical performance.

For short channel MOSFETs, the transfer characteristic curve changes more obviously than that for longer channel MOSFETs. A smaller gate voltage is required to increase the current initiation, indicating that the threshold voltage is significantly reduced, and the drain current changes more obviously at lower gate voltages (the curve slope is larger). In the saturation region, the drain current no longer shows a steady trend, which shows a strong leakage current leakage. For the switching characteristics of MOS, the short-channel effect degrades the sub-threshold performance and thus the switching performance.

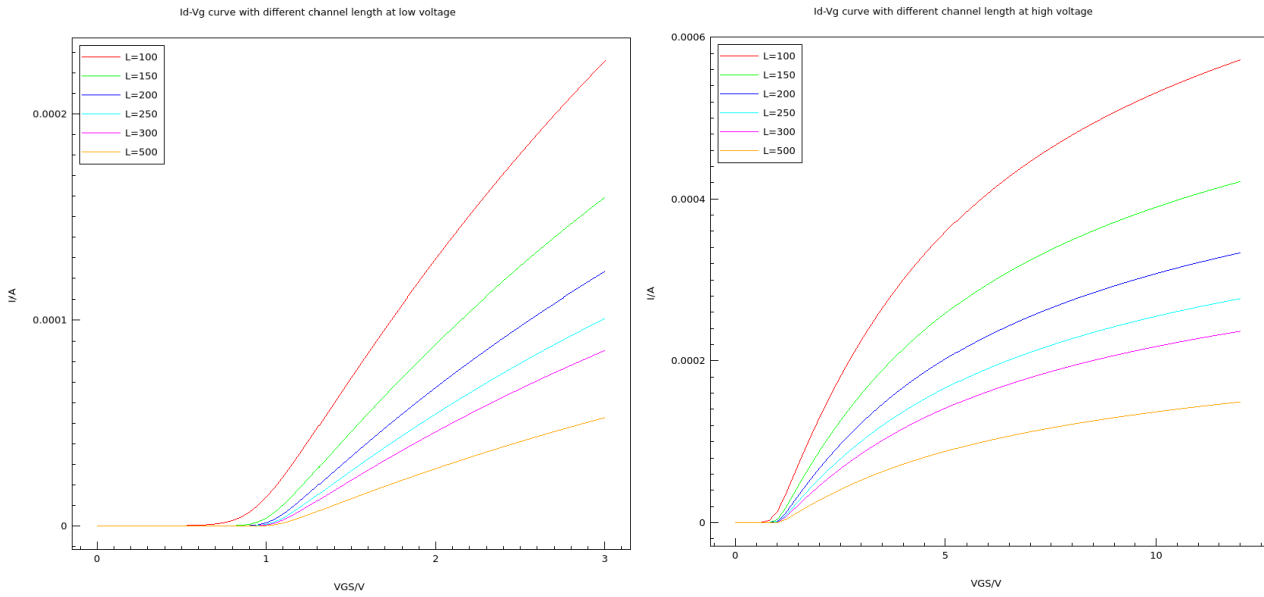


Figure 3: Comparison of transfer characteristic curves at low and high gate voltage

According to the simulation results, the effects of short channel effect on MOS tubes can be summarized as follows:

1. Threshold voltage drop: As the channel length decreases, the lower voltage required for conduction leads to a weakening of the gate voltage's ability to control the channel, thus affecting the switching performance.

2. Drain current increase: As the slope of the transfer characteristic curve changes, it can be concluded from the figure that the leakage current of short-channel MOS devices is easier to increase than that of long-channel MOS devices. Its subthreshold performance decreased significantly. At high grid voltage, this phenomenon is more significant, resulting in increased power consumption.

3. Intensify the channel length modulation effect: the leakage current in the transistor working area is more dependent on the regulation of the drain-source voltage V_{DS} , which affects the transconductance.

3.2. Potential distribution

Based on devices with different channel lengths, the potential distribution curves are analyzed experimentally. In the experiment, C1 line near the gate surface (0.005nm away from the oxide layer) and C2 line inside the channel (0.028nm away from the oxide layer) were selected to analyze the potential distribution in the channel as shown in Fig.4. The results show that the potential distribution of all MOSFET devices is a "potential well".

Influence of channel length on potential distribution:

According to Fig.5 and 6, the following conclusions can be drawn:

1. Short channel device: the potential drops faster in the middle of the channel (near $X=0$), indicating higher electric field strength. The minimum potential value at the center of the channel (bottom of the potential well) is relatively high, indicating that the drain electric field (DIBL effect) significantly affects the barrier height of the source pole, resulting in the reduction of the threshold voltage.

2. long channel device: the potential in the middle of the channel drops slowly, the electric field distribution is more uniform, and the potential change is more gentle. The minimum potential value of the channel center is lower, the potential barrier is more obvious, indicating that the gate has

stronger control ability of the channel, and the drain electric field has less influence. In addition, compared with short-channel devices, the potential distribution is more symmetrical, and the drain side is less affected by the drain voltage.

The potential distribution is also different for different locations. Those at the junction of gate oxide layer (C1 line) are directly affected by gate voltage V_{GS} , and have stronger regulation ability on the channel surface potential, and the overall potential is higher. On the curve, the barrier is steeper; The potential drops less in the channel. However, the position of channel center away from the gate oxide layer is more affected by the source leakage field and doping, and the control ability of gate voltage is reduced. In the short-channel device, the drain electric field (DIBL) significantly raises the potential on the drain side, resulting in an asymmetric barrier. At the same time, it is precisely because of this, the device has a larger barrier difference, and the short channel effect is more significant.

Physical mechanism: The control ability of gate voltage in the channel location away from gate oxide decreases exponentially due to the attenuation of the electric field of gate medium. The source-drain voltage at the center of the channel is more easily penetrated in the horizontal direction, which makes the potential distribution of the device asymmetrical. In addition, substrate bias may also have an effect on the barrier asymmetry. The influence of the potential distribution at different positions in the channel on the device performance is shown in Table 1.

Table 1: The influence of the potential distribution at different positions in the channel on the device performance

Characteristic	Near Gate Oxide Interface	Channel Center
Channel Center Threshold Voltage Control	Dominated by gate field; stable V_{th}	Influenced by drain/body potential; V_{th} prone to drift
Short-Channel Effects (SCE)	Partially shielded by gate field	Severe (DIBL, charge sharing)
Leakage Current	Governed by surface inversion layer	Additional bulk leakage paths may emerge
Drive Current	Governed by surface inversion layer	Minor contribution
Field Distribution	High vertical gate field	Strong lateral drain field (DIBL)

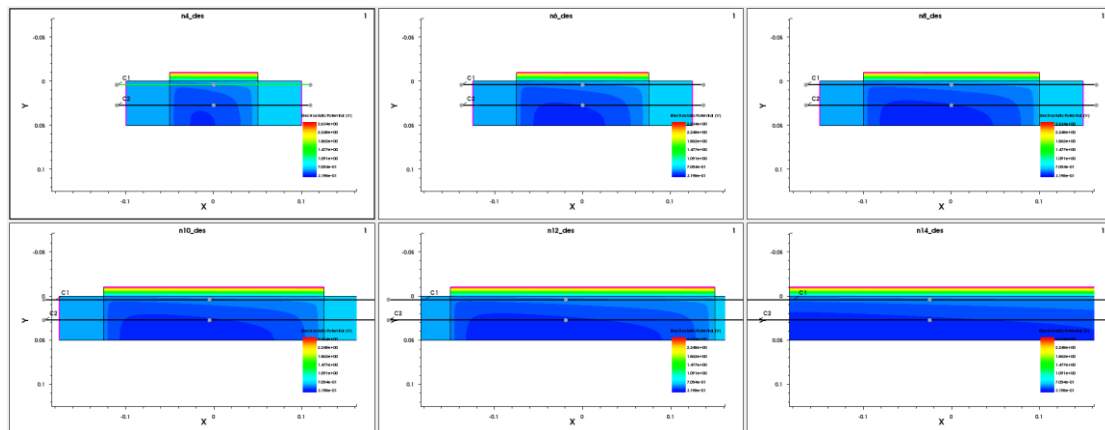


Figure 4: Schematic diagram of two selected line

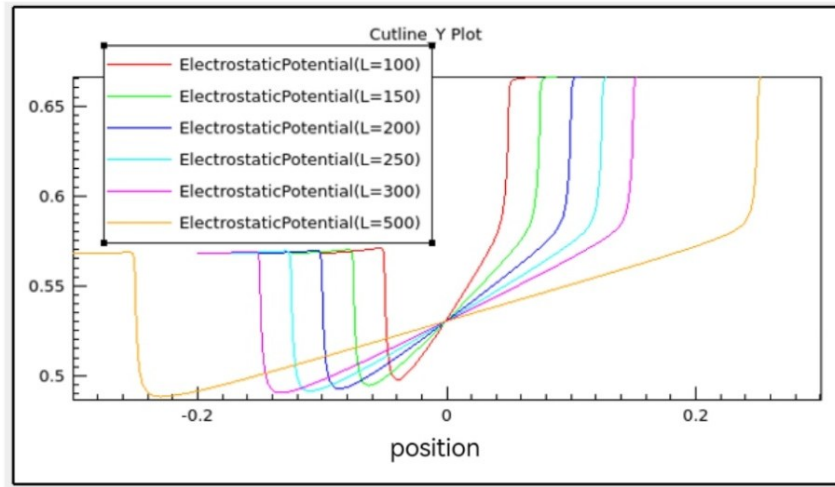


Figure 5: Electrostatic potential of the surface(0.005nm)

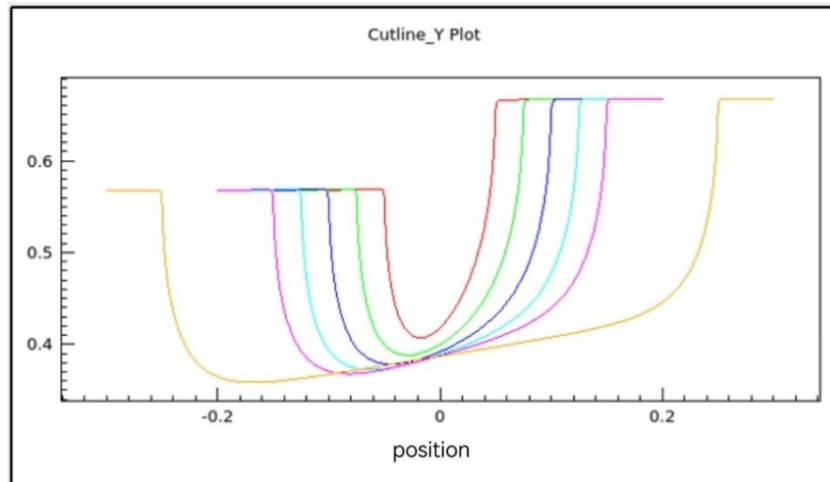


Figure 6: Electrostatic potential of the interior(0.028nm)

3.3. Electric field distribution

All the curves show the peak electric field near the source-drain junction, and the typical peak position is $x \approx \pm 0.15L$

When $L=100\text{nm}$, the peak electric field reaches $4.8 \times 10^5 \text{V/cm}$, which is 2.3 times higher than that when $L=500\text{nm}$.

When the channel length L is reduced from 500nm to 100nm , the peak electric field increases by 128% and the field bimodal distance decreases by 80% as shown in the following table 2.

Table 2: The relationship between the peak electric field and the double-peak spacing with the channel length of MOSFET

1. Channel length(nm)	2. Peak electric field(V/cm)	3. Bimodal distance(nm)
100	2.1×10^5	75
500	2.4×10^5	375

The grid charge control ratio is:

$$\frac{Q_{gate}}{Q_{total}} = 1 - \frac{2x_j}{L} \times \ln\left(\frac{L}{t_{ox}}\right) \quad (t_{ox} \text{ is the oxide layer thickness}) \quad (5)$$

The calculation results show that the proportion of gate charge control is 89% when $L=500\text{nm}$, and the proportion of gate charge control is reduced to 43% when $L=100\text{nm}$. This shows that with the shortening of channel length, the proportion of gate charge decreases, which leads to the decrease of threshold voltage, and the short channel effect is more significant.

The electric field distribution at the channel center decreases to 30% of the voltage at the channel surface, as shown in Fig.7, compared with Fig.8, and the peak value on both sides increases to $2 \times 10^5 \sim 3 \times 10^5 \text{V/cm}$. The general trend is consistent with that at the channel surface, reflecting the characteristics of low threshold voltage and barrier region compression of short-channel MOS devices.

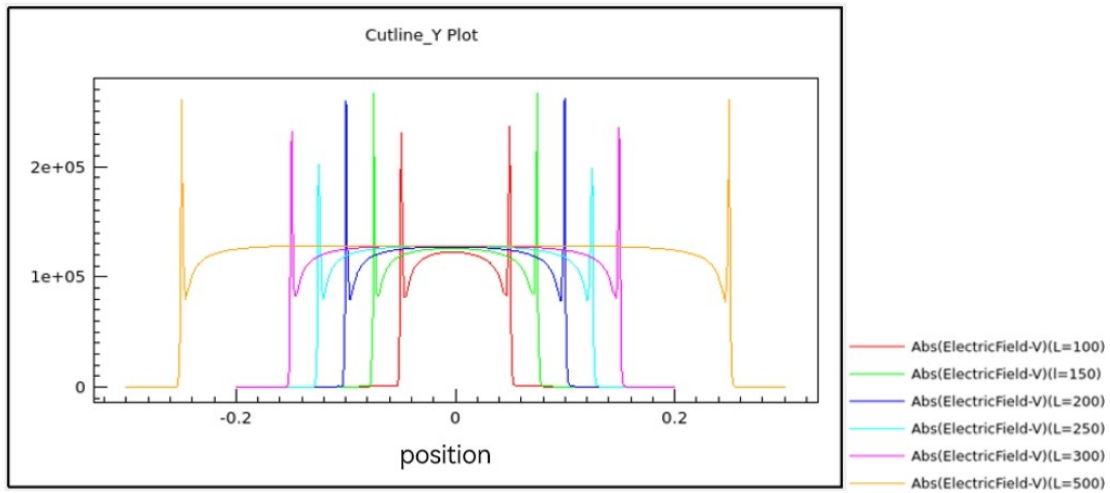


Figure 7: Electric field distribution of the surface(0.005nm)

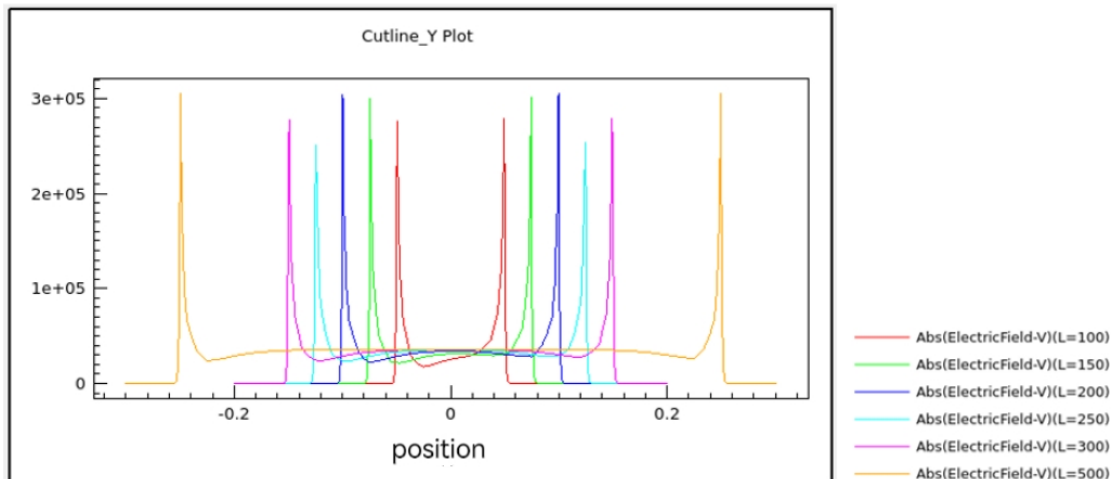


Figure 8: Electric field distribution of the interior(0.028nm)

4. Conclusion

In the development of MOS technology, in order to meet the needs of miniaturization of integrated circuits, the channel length of MOSFET is continuously shortened, which leads to short channel effect.

Through theoretical analysis and experimental design and simulation of Sentaurus TCAD, this study comprehensively explored the MOS design of different channel lengths and the principle of short channel effect. The short channel effect is mainly due to the decrease of channel length, which makes the source-drain PN junction affect the charge distribution under the gate oxide layer, and then lead to the decrease of threshold voltage. At the same time, it also causes the increase of drain current, the enhancement of channel length modulation effect and the decrease of sub-threshold performance, which have a negative impact on the switching performance of MOS devices. Through the design of MOSFETs with different channel lengths and the analysis of their transfer characteristic curves, it is found that the long-channel devices have better control ability of carriers and larger threshold voltage, and perform better in low-power applications and high-voltage circuits. In contrast, the transfer characteristic curve of short-channel devices changes more significantly, the threshold voltage is lower, and the leakage current problem is more serious. The effect of short channel effect is further confirmed by the simulation results of potential and electric field distribution. In short-channel devices, the potential in the channel drops faster, the electric field intensity is higher, and the gate-charge control ratio is reduced, which is consistent with the performance of the short-channel effect.

Therefore, understanding the short channel effect in MOS devices is crucial to the design and development of modern integrated circuits. As the demand for miniaturization continues to grow, it is necessary to find effective ways to mitigate the negative effects of short channel effects, such as using innovative device structures and advanced manufacturing processes. This will help improve the performance and reliability of MOS devices and promote the continued development of the semiconductor industry.

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