Proceedings of CONF-FMCE 2025 Symposium: Semantic Communication for Media Compression and Transmission
DOI: 10.54254/2755-2721/2025.GL27308

Unclamped Inductive Switching (UIS) Characteristics of GaN Power Devices: Mechanism, Testing, and Design Optimization

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Abstract. This paper systematically discusses the working principles, UIS testing methods, and structural optimization design of gallium nitride (GaN) power devices. First, the basic structure and operating mechanism of GaN devices are examined. The formation mechanism of the two-dimensional electron gas conductive channel in p-GaN HEMTs and the avalanche characteristics of vertical-structure devices are analyzed. Next, the UIS testing method is described, and the differences in test standards between traditional silicon devices and GaN devices are compared. Based on a study of failure mechanisms, a new p-GaN HEMT structure incorporating a p-type buried layer is tested. This structure significantly improves the UIS tolerance of the device by optimizing the electric field distribution, providing an effective solution to the reliability challenges of GaN power devices.

Keywords: gallium nitride, UIS, mechanism, testing, design optimization

1. Introduction

As a representative of third-generation semiconductors, gallium nitride (GaN) power devices have demonstrated significant potential in the field of power electronics due to their excellent material properties. Compared with traditional silicon-based devices, GaN devices exhibit higher electron mobility, larger critical breakdown electric fields, and lower conduction loss, making them particularly suitable for high-frequency and high-power-density applications, such as data center power supplies and fast-charging equipment [1]. However, in practical applications—especially under unclamped inductor switching (UIS) conditions—the reliability performance of GaN power devices differs significantly from that of silicon devices, which has become a key research focus. From the perspective of material properties, the advantages of GaN power devices are mainly reflected in the following aspects. First, their lateral device structures (such as p-GaN gate HEMTs) realize a two-dimensional electron gas (2DEG) conductive channel through the polarization effect, achieving extremely low on-resistance [2,3]. Second, GaN HEMTs on sapphire substrates exhibit unique self-enhancement characteristics under UIS conditions, where energy is dissipated by the collision ionization current, resulting in an actual withstand voltage lower than the theoretical resonance voltage [4]. In addition, vertical GaN PN diodes demonstrate a uniform current distribution in avalanche mode, and dynamic current flow can effectively disperse thermal stress,

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allowing the devices to withstand more than 5000 UIS pulses [5] [6]. In terms of extreme environmental adaptability, studies have shown that the UIS characteristics of p-GaN HEMTs at low temperatures are fully consistent with those at room temperature, and this temperature insensitivity confers particular advantages in aerospace applications [7]. By contrast, the avalanche capability of SiC devices is significantly reduced under the same conditions [7]. Although GaN power devices offer many advantages, several reliability challenges remain under UIS conditions. At the mechanism level, GaN devices lack the robust avalanche capability of traditional silicon devices, and their failure mechanisms manifest primarily in two modes. For lateral devices, the inverse piezoelectric effect induced by high electric fields can cause lattice cracks near the gate [2,8]. Vertical devices face the risk of electric field concentration at the edge terminal, with field plate delamination and dielectric layer cracking as the main failure modes [6]. Regarding performance degradation, repeated UIS stress can induce threshold voltage drift and abnormal changes in the dynamic on-resistance of p-GaN HEMTs, which is directly related to the filling of electron traps near the gate [9,3]. More critically, large current surges can exacerbate collision ionization and increase leakage current by more than an order of magnitude [3,10].

This paper is divided into four parts, with the main content of each part summarized as follows. The first part is the Introduction, which presents the advantages and existing challenges of gallium nitride (GaN) power devices and outlines the main objectives and organizational structure of this paper. The second part discusses the failure mechanisms of GaN power devices under unclamped inductive switching (UIS) conditions. The third part describes the UIS testing methods. The fourth part focuses on the optimization design of device structures.

2. Failure principle of gallium nitride UIS

Fig. 1 shows the cross-sectional diagram of the studied p-GaN HEMT structure [3]. The failure behavior of gallium nitride (GaN) power devices under unclamped inductor switching (UIS) stress exhibits a unique physical mechanism. When the energy accumulated in the load inductor of the circuit is transferred to the device, a transient high voltage is generated across the drain and source, causing the drain to become a high-potential terminal and forming a strong electric field directed toward the gate and source. Unlike silicon devices, GaN-based power HEMTs lack parasitic bipolar transistors, and their breakdown exhibits time- and voltage-dependent dielectric breakdown behavior. Specifically, the dynamic breakdown voltage is higher than the static breakdown voltage [1]. This special electric field distribution induces a significant potential difference within the p-GaN gate HEMT, triggering two key effects: first, the Schottky barrier formed by the gate metal and the p-GaN layer is forward-biased; second, the PIN structure composed of p-GaN/AlGaN/GaN is reverse-biased. In this context, the Schottky p-GaN contact blocks holes from flowing out of the gate region, whereas the p-GaN region in the Ohmic contact is short-circuited with the gate, allowing holes to flow out more easily, which results in stronger UIS tolerance for the Schottky contact [11]. This double-diode effect forms the core basis for understanding the UIS failure mechanism of GaN devices.

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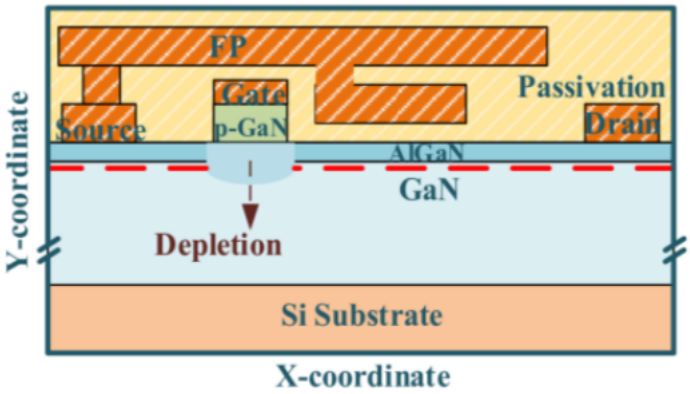


Figure 1. Cross-sectional diagram of the p-GaN HEMT structure

During the UIS voltage peak stage, the reverse-biased PIN structure undergoes significant changes. The p-GaN layer forms a negatively charged space-charge region, with its ionized acceptor concentration increasing by 20–25%, while a positively charged space-charge region is generated at the AlGaN/GaN interface, where the ionized donor concentration increases by 15–20%. High voltage also induces electron trapping near the gate and in the gate–drain region, further affecting the space-charge distribution [3]. This non-equilibrium charge distribution exhibits a persistent effect, maintaining a residual influence of microsecond-to-millisecond magnitude even after the UIS process concludes.

The threshold voltage change induced by UIS stress exhibits a typical three-stage characteristic. In the initial stage, the negative space charge in the p-GaN layer blocks the gate electric field, causing a positive threshold voltage drift ($\Delta V_{th} > 0$), typically ranging from +0.3 V to +0.8 V. In the intermediate recovery stage, holes gradually neutralize the negative space charge through diffusion and recombination. Simultaneously, for the electron–hole pairs generated by collision ionization under UIS stress, the electron detrapping rate is faster than that of the holes, increasing the density of the two-dimensional electron gas (2DEG) and reducing the on-resistance $R_{ds,on}$ by 5–15% [9]. Finally, due to the trapping of new holes by hole traps, a positive space-charge region is formed, leading to a negative threshold voltage drift ($\Delta V_{th} < 0$).

When the UIS process reaches the peak voltage, thermal excitation and collision ionization occur in the depletion region of the GaN channel layer, generating new electron–hole pairs. The electrons migrate toward the drain, while the holes move into the p-GaN barrier layer. In extreme cases, the extremely high electric field at the drain electrode (up to 12 MV/cm) can induce lattice cracks, resulting in a sudden increase in leakage current and localized burn-out [2]. Simultaneously, the high electric field may trigger the inverse piezoelectric effect, producing dislocations and defects that further exacerbate device failure [7].

After the UIS stress concludes, the non-equilibrium charge regions do not dissipate immediately, leading to a positive drift of the threshold voltage when the device is turned on. Over time, holes gradually recombine with the negative space charges; however, some holes become trapped, forming a positive space-charge region and resulting in a negative threshold voltage drift. Repeated UIS stress increases the number of holes captured by traps, reduces the magnitude of the positive drift, and accentuates the negative drift, consistent with the mechanisms of defect generation and

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enhanced charge-trapping under repeated stress [12]. These findings provide an important theoretical basis for understanding the reliability degradation of GaN power devices.

3. Gallium nitride UIS test method

The unclamped inductor switching (UIS) test method for gallium nitride (GaN) power devices involves a unique test procedure and specific parameter-setting requirements. Fig. 2 shows the schematic of the UIS test circuit for GaN E-HEMTs [11]. The complete UIS test process can be divided into four characteristic stages: the inductive energy storage stage, the energy transfer stage, the third-quadrant conduction stage, and the LC resonance stage. While the UIS test for traditional silicon MOSFETs follows the JESD24-5 standard, GaN devices require new test methodologies due to differences in physical structure. During testing, the relationship between the reverse-bias current (I_d) and the drain–source voltage (V_{ds}) is observed [1]. This four-stage test process fundamentally differs from the avalanche process of conventional silicon-based devices, necessitating a specialized testing scheme to accurately evaluate the UIS tolerance of GaN devices.

In terms of standard test environment settings, the basic configuration includes constant ambient temperature, power supply voltage, and load inductance. For example, a 50 V DC power supply is used, and the stress conditions are adjusted by varying the load inductance (10–80 μH) [11]. The device turn-on time is controlled at microsecond resolution by precisely adjusting the duty cycle of the driving signal, enabling accurate control of both inductive energy storage and UIS stress intensity. The test system typically consists of the inductor, DC power supply, capacitor, and driving circuit. In some experiments, current shunts are employed for board-level current measurements [11]. Test data indicate that characteristic failure waveforms appear in devices with different structures under specific conditions. These parameters serve as important benchmarks for evaluating the UIS reliability of GaN devices.

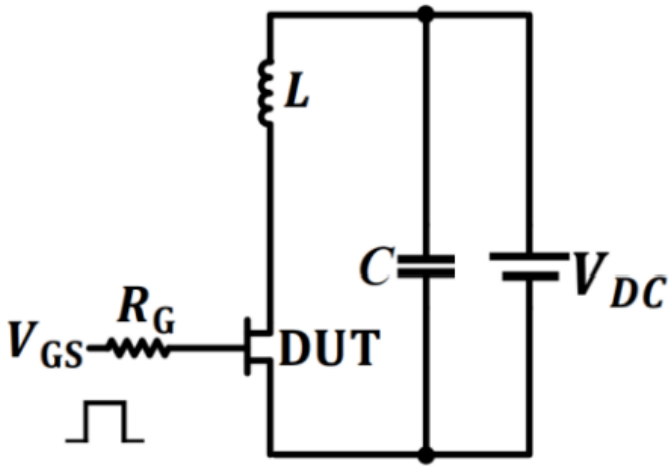


Figure 2. Schematic of the UIS test circuit

The systematic test scheme for enhanced GaN devices comprises two key components: a single UIS test under multiple inductance conditions and a parallel-device test under fixed inductance conditions. The test system employs standardized charging capacitors and precision shunt resistors to ensure accurate current measurements. In some experiments, the single-board UIS circuit is combined with a double-pulse test (DPT), allowing different stages to be controlled via timing

DOI: 10.54254/2755-2721/2025.GL27308

signals and enabling the measurement of dynamic parameters after an adjustable recovery period [9]. This multi-parameter combined testing method provides a comprehensive characterization of the failure behavior of GaN devices under various stress conditions.

The high-temperature UIS test scheme incorporates a precise temperature control system based on the standard test, ensuring temperature uniformity through constant temperature maintenance. For example, tests can be conducted in high-temperature environments, such as 150 °C [2]. Each test condition is repeated multiple times to eliminate random errors. This high-temperature testing method is particularly suitable for evaluating the reliability performance of GaN devices under harsh environmental conditions.

Regarding test parameter optimization, it has been found that the inductor energy storage can be accurately controlled by adjusting the duty cycle of the drive circuit's output voltage—for example, setting the duty cycle to 1% to prevent heat accumulation [3]. By monitoring waveform changes in real time and combining this with multi-terminal measurements, the device failure state can be accurately assessed, and the failure location can be preliminarily identified. Furthermore, device tolerance can be quantitatively evaluated by calculating parameters such as avalanche energy (E_{AS}) [13]. This method provides reliable experimental data for investigating the UIS failure mechanisms of GaN devices.

It is noteworthy that the UIS test results of GaN devices exhibit a significant dependence on device structure, with fundamental differences in the energy dissipation mechanisms among devices with different architectures. For example, GaN devices on sapphire substrates display voltage sags and current spikes during testing [4], which contrasts with the behavior of devices on silicon substrates. Additionally, the influence of temperature on test results cannot be overlooked. UIS test data obtained under high-temperature conditions provide an important reference for evaluating practical device performance.

4. Optimized design of device structure

Based on an in-depth understanding of the UIS failure mechanisms in p-GaN HEMT devices, this study proposes an innovative device structure optimization scheme. As shown in Fig. 3, the internal electric field distribution of the device under repeated UIS stress is significantly improved by introducing a p-type buried layer beneath the drain and connecting it to the drain. The core of this optimization strategy is to use the p-type buried layer to regulate the potential distribution within the device, thereby effectively reducing current density and surge voltage peaks in the channel region, ultimately enhancing the UIS tolerance of the device.

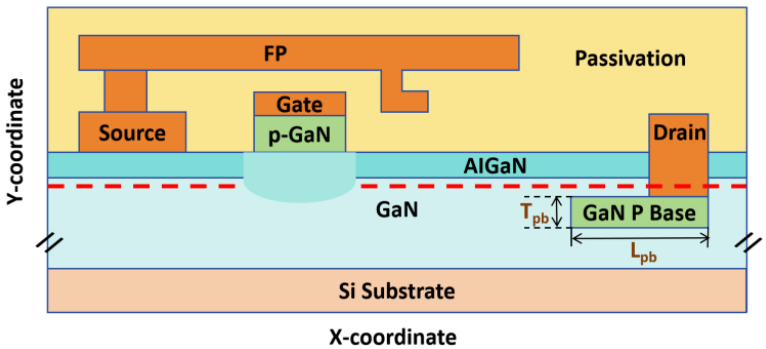


Figure 3. Improved structure of p-GaN HEMT device

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Simulation results indicate that the geometric parameters of the p-type buried layer significantly affect device performance. When the buried layer thickness is held constant, the breakdown voltage (BV) of the device increases with increasing buried layer width, but the on-resistance (R_{ds,on}) also rises. Similarly, for a fixed buried layer width, increasing the buried layer thickness can enhance the breakdown voltage, but it may also degrade the on-resistance. Through systematic optimization, a p-type buried layer structure with specific geometric dimensions is determined, maintaining the on-resistance within a reasonable range while ensuring breakdown voltage stability.

Improving the electric field distribution and temperature characteristics is the key mechanism for optimizing device structure and enhancing UIS performance. Compared with the traditional design, the optimized structure significantly reduces the longitudinal electric field intensity on the channel surface, particularly near the drain. At the same time, simulation results confirm that the lattice peak temperature of the optimized structure under UIS stress is substantially lower. This dual improvement in electric field and temperature distribution effectively alleviates the electrothermal stress on the device during the UIS process, thereby greatly enhancing reliability. Comparative test results further validate the effectiveness of the optimized design. The optimized structure demonstrates superior electrical properties under identical UIS stress conditions. Specifically, the optimized device can withstand higher UIS stress levels while maintaining stable performance parameters after multiple stress cycles. This improvement is primarily attributed to the re-regulation of the internal potential distribution by the p-type buried layer and the resulting electric field homogenization.

In-depth analysis indicates that the introduction of a p-type buried layer modifies the charge transport path in traditional p-GaN HEMT devices. During the UIS process, the buried layer structure provides additional conduction channels for carriers, effectively dispersing the high electric field region that is concentrated at the gate edge in conventional structures. Optimizing the charge transport path not only reduces the local electric field intensity but also improves the device's heat distribution characteristics, thereby achieving an overall enhancement of UIS tolerance.

It is noteworthy that the optimized design not only enhances UIS performance but also requires careful consideration of other key device parameters. Simulation results indicate that although introducing the p-type buried layer slightly increases the on-resistance, a favorable balance between breakdown voltage and on-resistance can be achieved by precisely controlling the geometric parameters of the buried layer. This parameter-optimization strategy provides an important reference for designing high-performance GaN power devices.

5. Conclusion

This paper systematically examines the working principles of gallium nitride (GaN) power devices, the unclamped inductor switching (UIS) test methodology, and the optimized design of device structures. Regarding device operation, the formation mechanism of the two-dimensional electron gas (2DEG) conductive channel in p-GaN gate HEMTs is analyzed, and the high-concentration electron accumulation induced by the interface polarization effect of the AlGaN/GaN heterojunction is clarified. Additionally, the avalanche breakdown characteristics of vertical GaN devices are discussed, highlighting that uniform current distribution can significantly enhance UIS tolerance. At the testing level, the fundamental differences between traditional silicon-based devices and GaN devices in UIS tests are detailed. Based on an in-depth study of failure mechanisms, an innovative p-GaN HEMT structure integrated with a p-type buried layer is proposed. This design effectively suppresses carrier injection in high-field regions by precisely regulating the longitudinal electric

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field distribution, providing a feasible technical approach for addressing the reliability challenges of GaN power devices under harsh conditions. Overall, this study establishes a theoretical framework for evaluating the reliability of GaN devices and offers an important reference for the design of next-generation high-performance power electronic devices.

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