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Research Progress of Carbon Nanotubes in Integrated Circuits

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Abstract. As the integrated circuit process enters the node below 7nm, Moore's Law approaches the physical limit. Carbon nanotubes (CNTs) have become the ideal channel materials in the post-molecular era due to their one-dimensional nanoscale structure, ultra-high carrier mobility, and excellent mechanical flexibility. This paper systematically reviews the research progress of carbon nanotubes in integrated circuits. First, this paper analyzes the chirality dependence of semiconductor carbon nanotubes and the challenges of ultra-high purity preparation, and focuses on the polymer purification and self-assembly technology to achieve wafer-level high-density arrays. Secondly, this paper discusses the performance advantages of carbon nanotube field-effect transistors in logic devices (such as ternary gate circuits, adders), memory, and fin field-effect transistor architecture. Finally, this paper analyzes the potential of carbon nanotubes in interconnection technology. Its current carrying capacity and thermal conductivity are significantly better than copper interconnection. Although there are still challenges in the large-scale preparation and integration process of carbon nanotube technology, it is expected to promote the practical application of carbon-based electronics through heterogeneous integration and 3D architecture innovation.

Keywords: carbon nanotubes, carbon nanotube field-effect transistors, integrated circuits

1. Introduction

An integrated circuit is a kind of microelectronic device that uses a semiconductor wafer as the carrier to interconnect and package the electronic components required by the circuit through a certain process. The smallest structural unit of a mainstream integrated circuit chip is a silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) Field-Effect Transistor (FET). The operating principle of FET is based on voltage control mechanism. Specifically, the voltage applied on the gate can adjust and control the carrier distribution density in the semiconductor channel. This change in carrier concentration directly determines the on-off and magnitude of the current between the source and drain, so that the FET plays a role in regulating the current path by voltage. The core of FET is the channel modulated by the gate, while the traditional FET channel is mainly composed of single-crystal silicon. However, as CMOS technology enters the node below 7nm, the traditional monocrystalline silicon FET will soon reach the physical limit of Moore's Law. Continuing to reduce the size of the technology node will significantly increase the cost. Therefore, it is a general

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trend to replace traditional silicon-based transistors with new materials. Carbon nanotube (CNT) has the characteristics of nanometer size, high carrier mobility, excellent mechanical flexibility, and its preparation process is compatible with existing silicon-based processes and equipment, reducing process development costs. Therefore, carbon nanotubes are considered to be the ideal choice for the next generation of transistor materials and have important research significance in the field of IC.

However, there are many challenges in the application of Carbon Nanotube Field-Effect Transistor (CNTFET). This paper will discuss the preparation of semiconductor carbon nanotubes, the application of CNTFET technology, and the application of carbon nanotube integrated technology. This paper aims to sort out the current application progress of carbon nanotransistors in the field of integrated circuits, point out the problems and challenges faced, and provide ideas for subsequent applications.

2. Characteristics and preparation of semiconductor carbon nanotubes

2.1. Material properties of semiconductor carbon nanotubes

CNT is a hollow cylindrical one-dimensional structure formed by curling a two-dimensional single-layer graphite sheet. Its structural configurations include the Zigzag, Armchair, and Chiral types. The remarkable difference in conductivity of carbon nanotubes is related to their chirality. The chirality of carbon nanotubes refers to the specific spiral arrangement of graphene sheets when they are rolled into tubes. This parameter determines the difference in the conductive properties of carbon nanotubes [1]. Chirality is usually represented by a pair of integers (n, m), that is, chirality index. This index is a vector to describe the way graphene lattice curls in a specific direction to form nanotubes. The chirality index (n, m) of carbon nanotubes is directly related to their helicity and electrical properties. When n=m, carbon nanotubes are called armchair nanotubes, and the chirality angle (helix angle) is 30 °; When n>m=0, carbon nanotubes are called zigzag nanotubes, and the chiral angle (helix angle) is 0 °; When n>m ≠ 0, it is called chiral carbon nanotubes. According to the conductive properties of carbon nanotubes, they can be divided into metal carbon nanotubes (m-CNTs) and semiconductor carbon nanotubes (s-CNTs). When n-m=3k (k is an integer), the CNTs are m-CNTs. When n-m=3k ± 1, the CNTs are s-CNTs. M-CNTs have very high current-carrying capacity(>10^9 A/cm^2)and have very high potential in IC interconnect technologies. Semiconductor carbon nanotubes have an adjustable bandgap structure(Eg≈0.9/d eV), which makes them ideal channel materials for field effect transistors [1]. However, the basic requirements of integrated circuits for such materials are extremely high. The purity of semiconductor carbon nanotubes is more than 99.9999%, and they need to be uniformly arranged on the entire wafer in a monodisperse state with equal spacing (5-10nm). These two requirements need to be met at the same time, which challenges its preparation [1].

2.2. Preparation methods of semiconductor carbon nanotubes

In carbon nanotube electronics, semiconductor nanotubes are the basis of transistors. A key prerequisite for realizing mass production of carbon nanotube integrated circuits is to prepare ultra-high purity (semiconductor purity>99.9999%), directional arrangement, high density (100-200/μm) and large area uniform nanotube films. It is precisely because the bottleneck of material preparation has not been broken through for a long time that the actual performance of CNTFET and integrated circuits is poor, and the performance is one order of magnitude behind the silicon based technology of the same node, which has become the biggest technical bottleneck in this field. The research

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group of the Department of Electronics, School of Information Science and Technology, Peking University has developed a new purification and self-assembly method to prepare high-density and high-purity semiconductor array carbon nanotube materials. On this basis, the team for the first time realized transistors and circuits with performance superior to silicon-based CMOS technology with the same gate length, demonstrating the advantages of carbon tube electronics [2]. The research group used multiple polymer dispersion and purification technology to obtain ultra-high purity carbon tube solution, and combined with the dimension limited self alignment method, prepared carbon tube arrays with density of 120/μ m, semiconductor purity of 99.9995%, and diameter distribution of 1.45 ± 0.23 nm on a 4-inch substrate, thus meeting the requirements of ultra large scale carbon tube integrated circuits [2]. In recent years, the growth of full-wall carbon nanotubes with special chirality has made some progress.

However, catalyst design and growth kinetics are still key challenges, and the growth mechanism of chiral control is still unclear. Liu proved in one of his works that the arrangement of the properties of dense semiconductor carbon nanotubes and transistors exceeds the performance of transistors using traditional metal oxide semiconductor configurations based on silicon technology [3]. The above research shows that CNTFET may show better performance than traditional silicon-based devices due to its high integration density.

3. Application of CNTFET in transistor technology

3.1. Application of CNTFET in logic device

The trend of multiplying the number of transistors described by Moore's Law is encountering a bottleneck. As silicon based MOSFETs are subject to physical limits such as leakage, power consumption and decline of gate control ability when further miniaturization, the International Technology Roadmap for Semiconductors (ITRS) predicts that its size reduction will be difficult to continue in about five years. Carbon nanotubes have very high carrier mobility, which enables CNTFET to effectively suppress the short channel effect, showing better performance, scalability, and energy efficiency than Si-MOSFET. CNTFET is a kind of field-effect transistor that uses semiconductor carbon nanotubes as the conduction channel, and its source and drain are connected through the nanotube channel. The overall device structure of CNTFET is very similar to that of conventional MOSFET, not only the manufacturing process is almost the same, but also its current and voltage characteristics are comparable. The operation of the device is determined by the relationship between the gate voltage and the threshold voltage. When the gate voltage is below the threshold—defined as the minimum needed to activate the transistor—the drain current remains nearly zero. Once the gate voltage surpasses this threshold, a significant increase in drain current occurs. An important characteristic of CNTFET is that its threshold voltage is a function of the carbon nanotube's diameter. This diameter is defined by the chirality index (n, m). This means that the threshold voltage can be precisely set by simply selecting different chiral vectors to adjust the diameter of the nanotubes. This unique advantage makes CNTFET more attractive than traditional CMOS technology in the design and implementation of ternary logic circuits.

CNTFET is considered as a feasible scheme to develop logic gates (the basic building blocks of digital electronic systems). The efficiency of traditional adder design can be significantly enhanced by integrating it into the circuit. The core mechanism is that the threshold voltage of CNTFET is a function of the diameter of carbon nanotubes, and the diameter can be adjusted by the chiral vector (n, m). Samadi H and others have successfully realized a CNTFET ternary multiplexer with a power supply voltage as low as 0.9V and a channel length of 32nm by adjusting the diameter of the

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nanotubes [4]. Compared with the traditional design, the number of transistors is significantly reduced, the power consumption is reduced, and the delay and noise margin are improved. Furqan Zahoor et al. provided CNTFET with Resistive Random Access Memory (RRAM) as the design feature of nonvolatile ternary logic gates. Instead of using huge resistors to implement ternary logic gates, this design uses active loads, RRAM, and CNTFET. Advantages of the gate are demonstrated in metrics such as chip are, circuit density, fabrication complexity, and power efficiency when implementing ternary NAND, TNOR operations, and the standard ternary inverter (STI). The three methods show that the number of transistors has been reduced by 50% [5-8]. A key benefit of substituting the large resistor in the conventional circuit with a RRAM and CNTFET-based p-type active load is the achievement of a more compact footprint and enhanced operational performance. In RRAM, the resistance of devices will change with the application of voltage, and the design of the ternary inverter uses this RRAM function. The advantages of using CNTFET resistance characteristics based on RRAM and p-type in ternary logic gates include reducing the number of components and area overhead. In conclusion, the application of CNTFET in logic devices provides a promising development direction for the highly efficient digital systems in the post-Moore era.

3.2. Application of CNTFET in memory

With the continuous shrinking of semiconductor process feature size, leakage power consumption and device reliability have become the core problems to be solved in modern storage technology [9]. The technology of electronic components based on carbon nanotubes has been advancing steadily, such as switches, field effect transistors and sensors. This development trend is more obvious after the emergence of carbon nanotube memory devices, followed by many related research work to explore the storage function of CNTFET.

In order to solve the design problem of SRAM in submicron scale, Shrivastava et al. proposed CNTFET as an alternative technical solution. Their research evaluated the performance of a variety of CNTFET based SRAM cells (including 6T, 7T, 8T and 10T structures) at the 32nm process node, and compared them with traditional CMOS cells [10]. The results show that the SRAM composed of CNTFET is superior to CMOS in power consumption and delay index, which is mainly due to its inherent high driving current, excellent short channel effect suppression ability and excellent gate control characteristics. Taking 8T SRAM as an example, in terms of dynamic power consumption, CMOS power consumption is 0.22676mW, CNTFET power consumption is 21.77 μW, and the power consumption is reduced by 90.39%. In terms of delay, CMOS delay is 62.3ps, CNTFET delay is 3.89ps, and the delay is reduced by 93.71% [10]. In order to meet the growing demand for energy efficiency in the data center, Chauhan et al. successfully designed SRAM cells with both high efficiency and low power consumption based on carbon nanotube technology. This research gives full play to the material advantages of CNT, and significantly reduces the power consumption while improving the operating speed [11]. The performance comparison analysis further shows that this new SRAM unit has obvious advantages in energy efficiency and speed compared with the traditional design.

3.3. Application of CNTFET in fin field effect transistor (FinFET) technology

As metal oxide semiconductor field effect transistor (MOSFET) with traditional planar transistor structure is limited in 22nm process nodes, the industry is transitioning to FinFET on 22nm technology nodes. FinFETs demonstrate superior efficiency with minimal leakage power, outperforming planar designs, although they are hampered by manufacturing hurdles and more

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pronounced reliability issues than traditional MOSFETs. Since FinFET is close to the limit at the 3 nm node, the research focus is to develop new transistor configurations, and one of the most practical alternatives is CNTFET.

Carbon nanotube devices are cylindrical, which makes them better than FinFETs in terms of gate regulation and size reduction. Fluctuations in the thickness of the oxide layer have minimal impact on CNTFET operation. In contrast, these same variations can significantly alter the drive current characteristics of a FinFET. CNTFET has shown a leading position over CMOS in many performance parameters, including lower power consumption and delay, better power delay product and higher stability. Zhang et al. have conducted circuit level benchmark tests and compared CNT and silicon based FinFET under the 22nm process. The performance benchmarks for analysis are propagation delay, overall power consumption and energy delay product (EDP). Data shows that CNT FinFET has advantages in speed and EDP. Especially in low-voltage applications, the EDP advantage of CNT FinFET optimized by threshold voltage can be expanded to about 50 times that of silicon based devices, which indicates that it has broad application potential in integrated circuits [12].

4. CNT application in the integrated process

At present, semiconductor integrated circuit manufacturing technology has entered the 5nm node era. However, the reduction of feature size has led to a great challenge for the bottom-up development mode dominated by photolithography, and the manufacturing process will seriously restrict the further development and application of IC circuits. From the perspective of electrical performance, the reduction of feature size will lead to higher and higher current density carried by the internal conductor of IC circuit, especially when the manufacturing process enters 32nm, the current density carried by the circuit has reached 10 ^ 7A/cm2, which has exceeded the current density of copper, the main conductor material in IC circuit. Therefore, the possibility of electron migration in the circuit increases, which will increase the circuit temperature and affect the stability of the circuit, which will significantly reduce the life of devices made of semiconductor integrated circuits.

CNT interconnection technology provides an efficient connection scheme for integrated circuits. Its excellent electrical and mechanical properties make it show obvious advantages in traditional Cu interconnection technology. The electrons of CNT only propagate along the axial direction, which largely reduces the probability of scattering in the process of electron transport, making the carrier mobility that CNT can withstand more than 70% higher than that of silicon materials, and making the current density that CNT can withstand more than 1000 times higher than that of copper wires after interconnection [13]. CNT has good conductivity, with a conductivity of 10 ^ 6 S/m, which is much higher than that of copper (about 5.8 × 10 ^ 5 S/m). In the trend of size reduction, the superior thermal conductivity of CNT also greatly improves the thermal management problem and reduces the power consumption.

In terms of manufacturing process, chemical vapor deposition (CVD) is the mainstream CNT growth method in the industry. CVD is to decompose carbon-containing compounds to provide carbon sources, and then realize the growth of CNT under the role of catalysts (transition metal elements or their combination elements). This method can control the diameter and growth rate of CNT by adjusting the temperature and gas composition, and the growth rate is usually 50-100 μm/min. Li used low-energy O2 plasma instead of the chemical mechanical polishing process to open the port of MWCNT, and increased the electronic transport channel between MWCNT and metal to reduce its interface contact resistance while keeping the chemical state of the CNT tip free

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from pollution. The MWCNT treated with O2 isolators directly forms an ohmic contact with titanium silicide, and its interface contact resistivity is 1.83 μΩ· cm2. This contact mode is conducive to the transmission of information and energy from MWCNT to the outside world [14]. More importantly, this interconnection technology is compatible with CMOS technology, which can realize the assembly of CNT interconnects with high current density.

In recent years, CNTFET technology has made great progress, which makes it increasingly feasible to be an alternative to traditional CMOS devices due to its excellent performance and miniaturization potential. However, the technology still faces obstacles to large-scale commercial use, especially the key problems such as low-cost mass production and high-density integration. Because of this, a lot of theoretical and experimental research work is urgently needed in the future to deeply evaluate the potential of CNTFET in various application scenarios.

5. Conclusion

This article systematically analyzes the potential and challenges of carbon nanotubes in integrated circuits. Research shows that semiconductor carbon nanotubes are ideal channel materials for breaking through the physical limits of silicon-based CMOS technology by virtue of their nanoscale one-dimensional structure, ultra-high carrier mobility, and excellent electrical properties. Fabrication of high-density, high-purity semiconducting carbon nanotube arrays on a wafer scale has been achieved by leveraging polymer-based purification and self-assembly techniques, thereby paving the way for large-scale integration. At the device level, CNTFET has shown significant advantages in logic gate circuits, memory, and FinFET architectures, including performance improvements such as power consumption reduction of more than 90% and delay reduction of more than 90%. In the interconnection technology, carbon nanotubes show much higher current-carrying capacity and thermal conductivity than copper. Although there are still challenges in the large-scale preparation and integration process, carbon nanotube technology is expected to promote the application of carbon-based electronics in the post-Moore era and provide a new path for the development of the integrated circuit industry through heterogeneous integration and 3D architecture innovation.

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