Proceedings of the 3rd International Conference on Mechatronics and Smart Systems
DOI: 10.54254/2755-2721/2025.30623

Optimizing Power Efficiency in CMOS Image Sensors Control Circuits

Yehao Zhao[1†], Haowen Zheng[2†], Yuqiao Gu[3†], Fong-Ruei Chung[4*†]

[1]University of New South Wales, Australia
[2]University of Wisconsin-Madison, Madison, USA
[3]Suzhou Foreign Language School, Suzhou, China
[4]Manila Xiamen International School, Xiamen, China
**Corresponding Author. Email: raychung996@gmail.com*
[†]These authors contributed equally to this work and should be considered as co-first author.

Abstract. CMOS image sensor (CIS) control circuit has a non-negligible problem, which is the power efficiency. Research has shown that the power consumption of the CIS control circuit is affected mainly during the process of converting light to voltage signals. By reviewing the related research and products that use CIS control circuits, this study aims to find the current efficiency and flaws of the components in CIS control circuits to provide an optimized solution for each impediment. We separate different components in CIS control circuits and analyze each of them with corresponding efficiency and obstacles to increase efficiency. Subsequently, ideas and solutions for overcoming the challenges to increase the efficiency of components with certain trade-offs will be provided. Based on the analysis of each possible solution, the team recommended future development for these solutions that may optimize the efficiency of CMOS image sensors with minimal trade-offs.

Keywords: CMOS, CIS, Power Consumption, Optimize Efficiency

1. Introduction

This paper aims to study the power characteristics of CMOS image sensors and the feasibility of a power reduction scheme. As a product of the new era, the CMOS (complementary metal oxide semiconductor) image sensor (CIS) has gradually become an indispensable component in the imaging system of modern electronic equipment due to the extremely low energy consumption, highly integrated capability, and extremely fast data processing speed of CMOS [1]. CIS technology benefits various fields, such as consumer electronics, biomedical devices, and intelligent monitoring systems [2]. Compared to traditional imaging technologies, especially charge-coupled devices (CCD), it has lower power consumption, faster data reading speed, and is able to integrate all processing elements on a tiny single chip [3,4].

DOI: 10.54254/2755-2721/2025.30623

2. Primary power consuming components associated with the control circuit

As CIS technology continues to evolve, reducing power consumption as much as possible under maintaining performance becomes increasingly important. This report will examine the key components that improve power consumption in CMOS image sensors, highlight the specific applications of the corresponding components, and explore potential solutions to improve the energy efficiency of CIS control circuits.

2.1. Power efficiency of amplifier

The first is one of the most important power-consuming components in CMOS image sensors: amplifiers. An amplifier enhances the weak electrical signal of a photodiode sensor array [5], raising it to a sufficient level for subsequent circuits to process the signal. However, to ensure that the image sensor can capture the light signal in real time, the amplifier usually needs to run continuously, which inevitably greatly increases the system's power consumption [6]. Especially in systems for high-speed or high-resolution imaging, the power needs of amplifiers are particularly prominent. With the increasing demand for higher image resolution, more frames per second, and faster processing speed, the power consumption of amplifiers has reached 30% to 50% [7], which has become a complicated problem in the power optimization process.

2.2. Power consumption associated with focusing mechanisms

At the same time, the CMOS image sensor might autofocus while the system is running. The CIS-based autofocus system relies on the preprocessing mechanism of partial pixels. During the focusing process, some pixels will be called at any time to judge the object distance to ensure that the sensor can adjust the focal length quickly and accurately under different shooting conditions to maintain the best image clarity. Therefore, the high-speed focusing mechanism needs to mobilize a lot of electricity and computing power to achieve this function. In a dynamic shooting environment, frequent focal length adjustment will further increase the system's power consumption [8]. For applications that require fast response, such as video recording or tracking moving objects, this additional power consumption can significantly negatively impact device battery life.

2.3. Power consumption associated with image stabilizing capacitor

In addition, the image stabilization system is also a power-consuming component in modern CMOS image sensors. Most of the time, CMOS image systems use stabilization systems to reduce image blurring caused by camera shake or the movement of the subject during photography. In order to achieve adequate image stabilization, the capacitors within the sensor must undergo frequent charging and discharging operations during image capture [9]. The capacitor's large capacitance value can ensure the system's stability but also lead to high energy consumption. When using high-resolution applications such as high-resolution video recording, the power consumption of the image stabilization system can account for 10–30% of the overall power consumption [10]. With the increasing demand of users for higher image quality, the power consumption of image stabilization systems is becoming more and more prominent, and it has become one of the critical factors in power optimization and design.

To sum up, although the CMOS image sensor has obvious technical advantages in many aspects, the amplifier, autofocus mechanism, and image stabilization system in its internal control circuit will still produce the corresponding power consumption problem in a higher resolution environment and

DOI: 10.54254/2755-2721/2025.30623

large amounts of data recording. Considering the increased challenge, the following pages will propose some optimization and innovation of circuit design and power management techniques to balance power consumption and performance.

3. Potential solutions to reduce the power consumption of CMOS image sensors

Reducing the power consumption of CMOS image sensors requires a combination of advanced circuit design and innovative power management strategies. In response to the growing demand for energy efficiency and high performance, researchers and engineers have explored various potential technical approaches to minimize power consumption while ensuring that sensors do not compromise performance in high-speed and high-resolution applications. Several major solutions are explored in detail below. Each of these approaches has advantages and disadvantages in real-world applications, and trade-offs must be made based on specific scenarios.

3.1. Reduce the operating voltage

The first method is to reduce the operating voltage of the system, which is one of the most effective ways to reduce power consumption. Since the power consumption of a circuit varies with the square of the voltage when the system resistance is held constant, even a tiny reduction in voltage will result in a significant offset in power consumption. However, lowering the voltage is not a perfect solution. Lower operating voltages may affect the efficiency of CMOS image sensors, and lowering the supply voltage may lead to performance bottlenecks when improving system response times [11], such as in real-time imaging or high-definition video capture. So when high-speed data processing is required, the system needs to automatically recognize and increase the voltage; this solution puts specific requirements on the software algorithm [12].

3.2. Using power gating technology

Power gating is another potentially effective method of power consumption optimization. Systems with power gating reduce static power consumption by selectively shutting down parts of the circuitry that are not in use during operation [13]. Power gating is more effective than standard power supply methods in systems with idle duty cycles [14]. For example, during the focusing process, the system only needs partial pixels to focus and temporarily turns off the rest of the pixels to reduce static power consumption. Power gating can also significantly reduce leakage current [15], especially in CMOS systems using deep sub-micron processes, which can significantly improve system power performance. When power gating is enabled, system behaviors do not affect sensor performance. The circuit can start when there is a performance requirement to restore full functionality. This approach is, therefore, well suited for image sensor systems that operate intermittently.

3.3. Reducing the capacitance

In addition, to ensure the stability of the circuitry during image capture, the control circuitry of CMOS image sensors often needs lots of large capacitors, so reducing the number of capacitors in the control circuitry may reduce the power consumption [16]. Large capacitors can consume a lot of energy during charging and discharging, especially when frequently capturing high-frame rate images. Therefore, by optimizing the circuit design, reducing the number of capacitors in the circuit may reduce the energy required for charging and discharging and reduce the loss. At the same time,

DOI: 10.54254/2755-2721/2025.30623

reducing the number of capacitors can also reduce the capacitor charging and discharging time and improve the overall response speed of the circuit to enhance the overall stability of the circuit. Higher response speed is essential for high-speed imaging systems because delays in high-speed imaging systems may lead to degradation of image quality.

4. Future outlook

With the development of technology, CMOS sensors may reduce power consumption through more complex circuit design in the future. At the same time, more intelligent algorithms can achieve more accurate system voltages, and module switches control timing to reduce unnecessary energy loss [17].

However, combined with the current development trend, this paper is more inclined to CMOS image sensors in the future, which are more likely to rely on substantial advances in manufacturing processes to reduce power consumption because it is simpler to do so.

5. Conclusion

In summary, in this report, reducing power supply voltage, power supply gating, and reducing capacitance are the three main strategies for reducing the power consumption of CMOS image sensors. Each method has unique advantages and limitations according to specific needs in practical applications. As the technology advances, further optimization in these aspects will help CMOS image sensors achieve a better balance between power consumption and performance, promoting their continued application and development in various fields.

Acknowledgement

Yehao Zhao, Yuqiao Gu, Fong-Ruei Chung and Haowen Zheng contributed equally to this work and should be considered co-first authors.

References

[1] Bin Luo, Fuxing Yang and Lei Yan, "Key technologies and research development of CMOS image sensors, " 2010 Second IITA International Conference on Geoscience and Remote Sensing, Qingdao, 2010, pp. 322-325
[2] Wang, C. C. (2001). A study of CMOS technologies for image sensor applications (Doctoral dissertation, Massachusetts Institute of Technology).
[3] Wang, F., & Theuwissen, A. (2017). Linearity analysis of a CMOS image sensor. Electronic imaging, 29, 84-90.
[4] El-Desouki, M., Deen, M. J., Fang, Q., Liu, L., Tse, F., & Armstrong, D. (2009). CMOS image sensors for high speed applications. Sensors, 9(1), 430-444.
[5] Eynde, F.O., Sansen, W. (1993). The Power Consumption of CMOS Wideband Amplifiers. In: Analog Interfaces for Digital Signal Processing Systems. he Springer International Series In Engineering And Computer Science, vol 225. Springer, Boston, MA.
[6] K. -J. Kim, T. H. Lim and K. H. Ahn, "The novel high efficiency on chip transformers for the CMOS power amplifier, " Proceedings of the 2009 12th International Symposium on Integrated Circuits, Singapore, 2009, pp. 401-404
[7] IntechOpen. (n.d.).Power Consumption in CMOS Circuits.
[8] Choi, B. S., Jo, S. H., Bae, M., Kim, S. H., & Shin, J. K. (2016). A CMOS image sensor with variable frame rate for low-power operation. Electronic Imaging, 28, 1-4.
[9] Shauly, E. N. (2012). CMOS Leakage and Power Reduction in Transistors and Circuits: Process and Layout Considerations. Journal of Low Power Electronics and Applications, 2(1), 1-29
[10] Yeh, C. N., & Lai, Y. T. (2006, May). Low power readout control circuit for high resolution CMOS image sensor. In 2006 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 4-pp). IEEE.

DOI: 10.54254/2755-2721/2025.30623

[11] A. U. Diril, Y. S. Dhillon, A. Chatterjee and A. D. Singh, "Level-shifter free design of low power dual supply voltage CMOS circuits using dual threshold voltages, " in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 9, pp. 1103-1107
[12] Y. -C. Hung, Jian-Cheng Chen, Shao-Hui Shieh and Chiou-Kou Tung, "A survey of low-voltage low-power technique and challenge for CMOS signal processing circuits, " Proceedings of the 2009 12th International Symposium on Integrated Circuits, Singapore, 2009, pp. 554-557 [1] Park, J. C., & Mooney III, V. J. (2006). Sleepy stack leakage reduction. IEEE transactions on very large scale integration (vlsi) systems, 14(11), 1250-1263.
[13] Choi, J. (2016, October). Review of low power image sensors for always-on imaging. In 2016 International SoC Design Conference (ISOCC) (pp. 11-12). IEEE.
[14] Leong, P. H. W., Cheung, R.C.C., & Hou, Y. H. (2015). Ultra-Low Power CMOS Image Sensor with On-Chip Energy Harvesting. Sensors, 15(3), 5531-5553
[15] Jeon, B. K., Hong, S. K., & Kwon, O. K. (2016, October). A low-power 10-bit single-slope ADC using power gating and multi-clocks for CMOS image sensors. In 2016 International SoC Design Conference (ISOCC) (pp. 257-258). IEEE.
[16] Y. -W. Hsiao and M. -D. Ker, "Bond Pad Design With Low Capacitance in CMOS Technology for RF Applications, " in IEEE Electron Device Letters, vol. 28, no. 1, pp. 68-70, Jan. 2007
[17] N. Ogino et al., "Development of an FPGA-based Readout System of CMOS Image Sensor toward Future Satellite Missions, " 2021 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Piscataway, NJ, USA, 2021, pp. 1-2