Proceedings of CONF-FMCE 2025 Symposium: Semantic Communication for Media Compression and Transmission
DOI: 10.54254/2755-2721/2025.GL30920

A Review of Power Optimization Strategy Based on Clock-Gating Technology

Yutong Cai[1*], Youruo Hu[1], Changrui Liu[2]

[1]*Wuhan Britain-China School, Wuhan, China*
[2]*QSI International School of Shenzhen, Shenzhen, China*
**Corresponding Author. Email: 201802188@qq.com*

Abstract. Complementary Metal-Oxide Semiconductor (CMOS) integrated circuit technologies are advancing, with mature circuit designs and developed components; inevitably, the power consumption increased dramatically. Yet, an outstanding technique, clock-gating, can effectively reduce dynamic power consumption in CMOS circuits. This paper mainly focuses on the dynamic power consumption of CMOS, which can be optimized by specific technologies. The optimization strategy involved in this paper aimed at clock-gating technologies, which are widely used. This work tends to estimate the dynamic power consumption, an estimation based on simulation. Clock-gating technology is thenapplied in real life to validate the methods presented in the paper. For instance, the ISCAS'89 benchmark circuits and CPUs. Finally, this paper evaluates the clock-gating technique in CMOS integrated circuits and highlights its significance in power optimization. Although there are some limitations in the area of the clock net, these techniques can still effectively reduce power consumption in CMOS circuits and ensure power efficiency.

Keywords: CMOS integrated circuit, low-power consumption, dynamic power, power optimization strategy, clock gating technology

1. Introduction

A significant amount of research has been devoted to lowering the power consumption in CMOS integrated circuits, a type of microchip technology used in various digital devices. It can be characterized by its unique way of fabricating Integrated Circuits (ICs), using N-type and P-type Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) for logic functions. This device is vital to modern society due to its extensive application across the electronic field; for example, it is used in digital cameras, digital phones, computers, etc. Hence, further study to reduce power consumption in CMOS circuits should be conducted, which leads to the topic of this study: the use of clock-gating technology in CMOS.

Over the past few years, the topic of power optimization in CMOS has gained notable attention. Power optimization strategies focus on two sources: dynamic power and static power; however, this paper will mainly focus on dynamic power. Early research focused on a low-power CMOS amplifier [1], while later research stressed circuit improvement and plan mechanization strategies [2]. This study has shifted the focus to using clock gating technology, which disables the clock signal to

DOI: 10.54254/2755-2721/2025.GL30920

inactive parts of the circuit. This is achieved by implementing logic gates (clock gating cells) that control the clock signal to specific circuit components, shutting off the clock when not in use.

Nonetheless, only some studies focused on the low-power consumption of CMOS based on clock gating technology [3,4]. One of these studies contained several power optimization methods and mainly focused on static power [3]. Furthermore, neither of the remaining studies focused specifically on CMOS integrated circuits, nor does it provide specific strategies to decrease dynamic power consumption [4].

On this account, this paper aims to provide specific methodologies and an innovative perspective. Key contributions include the estimation of dynamic power consumption, optimization strategies for clock tree power reduction based on clock gating technology, and verifying proposed methods through real-life applications. To ensure relevance and credibility, this study uses data from recent practices and research (e.g., 2018-2025). Moreover, this study extends previous research by evaluating dynamic power consumption through the ISCAS'89 benchmark circuits (a type of circuit), with both simulation models and physical measurements. A case study on a low-power touch-based lifelogging processor (a low-power microprocessor that records and processes a person's activity data in real time) demonstrates the practical effect of the proposed methods. This paper provides a comprehensive review of power-efficient design strategies in CMOS integrated circuits.

2. Background

2.1. Dynamic power consumption

This analysis of power consumption is based on the fundamental CMOS inverter circuit depicted in Figure 1.

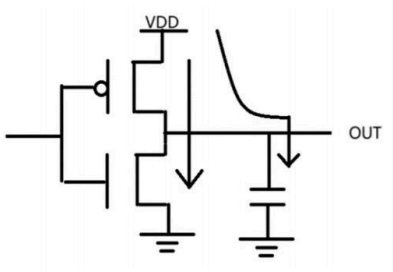

Figure 1. CMOS inverter circuit [5]

It is a common representation of switching power. The evidence and analysis suggest that the clock-gating technology is an effective method as it measurably reduces the activity of level transitions [5].

2.2. Dynamic estimation of power consumption

The dynamic estimation of power consumption is essentially an estimation based on simulation: using a method that involves a large number of input vectors to estimate the power consumption of the circuit according to different abstraction levels of the power consumption model. Simulating power consumption at different abstract levels entails a trade-off: higher accuracy demands greater computational resources, while lower abstraction levels are time-efficient but limit precision.

DOI: 10.54254/2755-2721/2025.GL30920

Therefore, in actual design, we need to balance computational accuracy and computational speed based on actual requirements, and adopt appropriate simulation techniques at different design stages.

Power consumption estimation requires adding a set of analog vectors at the original input end of the circuit. The selection of the input vectors mandates particular attention to two points: the samples of the input vectors should be exemplary and suitable for the current design. The size of the sample vector sequence set should be applicable: neither too large nor too small, too large will elevate the simulation time and too small will lead to insufficient accuracy of the estimation. The first issue mentioned above requires a wise selection of the input vectors; the second challenge can be resolved using the Monte Carlo method (computational algorithms that rely on repeated random sampling), which can properly address the obstacles of sample size and simulation stopping criteria [6].

2.3. The basic principle of clock-gating technology

To implement the clock-gating technique, additional logic is required to generate a clock-enable signal. This signal is activated exclusively when it reaches a logic "0" or "1"—a state determined by the specific design of the circuit—and this mechanism directly contributes to lowering dynamic power consumption.

The core objective of clock gating is to block unnecessary clock pulses from being transmitted to circuit components where the output remains unchanged. As shown in Figure 2, the circuit structure of clock gating consists of two parts: an "overall clock gating scheme" and a "single clock gating unit." This specialized circuit configuration is specifically applied to reduce dynamic power consumption in digital circuit systems.

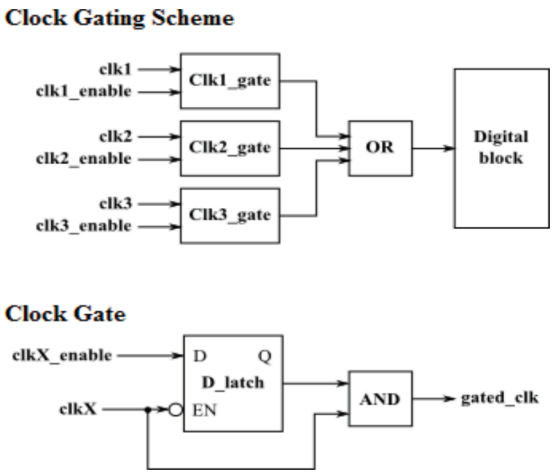

Figure 2. Clock gating [7]

3. Clock-gating circuit design

Clock gating technology is frequently employed in gate-level elements such as "AND", "OR", "NAND", and "NOR" gates. However, a drawback of gate-based clock gating technology is that during its usage, when a signal transitions from a low voltage level to a high voltage level, the rising transition time is longer than the falling transition time, which may result in glitches, as shown in Figure 3. The following 7 techniques suggest some possible solutions to handle these glitches.

DOI: 10.54254/2755-2721/2025.GL30920

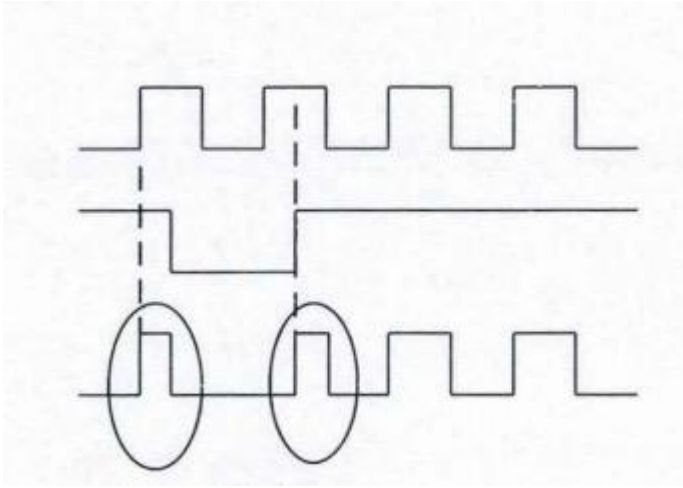

Figure 3. Glitches [6]

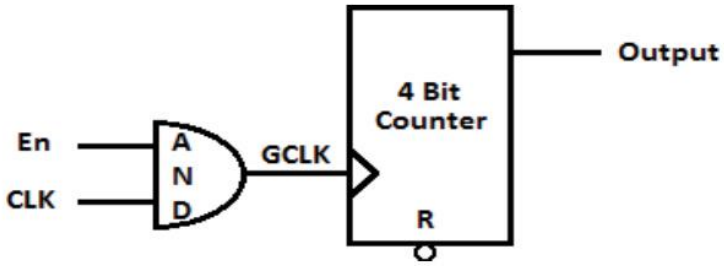

Figure 4. AND based clock gating [7]

3.1. AND gate

The AND gate is the most commonly used gate circuit for clock gating due to its simple logic [8]. To gate the clock, a dual-input AND gate can be inserted into a four-bit counter, with one input being the clock and the other input being the enable signal "En". Figure 4 shows a simple AND based clock gating. When the enable pin is at 1, the shorter falling time from high level to low level causes the counter to increment a count value when triggered by the negative edge. On the contrary, if the enable pin is equal to 1 at the positive edge, a larger falling time will occur, small gliches will be produced, and the resulting output will have an error [7].

As a general principle, the AND gate functions to support negative-edge triggering. Only when both inputs reach high level will the "AND" gate be enabled [8].

3.2. Clock gating based on latches

Latch-based clock gating refers to the configuration where a level-sensitive latch operates with a clock signal governed by an enable pin. The clock pulse with a managed enable signal, as presented in Figure 5, is transmitted to the AND gate embedded in the latch-based clock gating module.

The change in the enable pin occurs during the negative clock cycle, while the output remains unchanged during the positive clock pulse. During activation, changes in the enable signal can be observed during the negative clock cycle. During the sleep period of the positive cycle, changes in the enable signal can cause some errors, but it does not result in a mismatch with the delay between the clock and the enable signal [7]. The number of transistors used to build digital units is closely

DOI: 10.54254/2755-2721/2025.GL30920

related to their complexity, as the number of transistors need to build a latch is less than that required to build a flip-flop [9]. In the clock gating mechanism based on latches, glitches can be avoided, but this approach will lead to an increase in latency due to the impact on time verification.

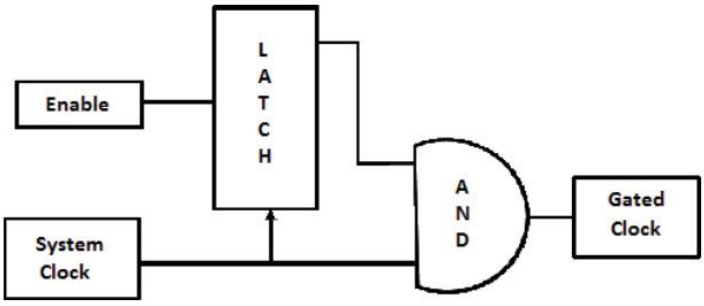

Figure 5. Latch based clock gating [7]

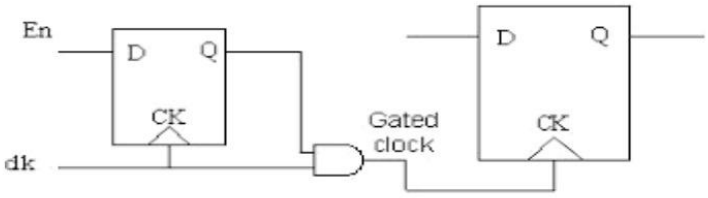

Figure 6. Flip-flop based clock gating [7]

3.3. Clock gating that relies on flip-flops

Clock gating implemented with flip-flops relies on edge-triggered flip-flops to regulate the clock enable pin, sharing similarities with latch-based clock gating architectures. As illustrated in Figure 6 (referenced above), this flip-flop-based clock gating scheme operates by using "AND" gates and the enable signal to control a D flip-flop. Notably, this flip-flop-based design exhibits two key drawbacks: it has an extended sleep duration and is more vulnerable to glitch interference. Additionally, during switching operations, the flip-flop requires a larger capacitor to complete charge and discharge cycles. This larger capacitance directly leads to significant dynamic power consumption. Over time, these issues collectively result in heightened circuit design complexity and compromised overall performance. For these reasons, flip-flop-based clock gating has also failed to gain widespread adoption in practical applications [7].

3.4. Synthesis-driven clock gating

The clock enable signal is set at the system level. When the circuit does not require a clock, the switching activities of a certain functional module in the system clock domain are redundant and consume most of the system power. To solve the problem, it is possible to effectively define and capture the cycle of a specific functional module, and introduce a method called data-driven clock gating [7]. The core of data-driven clock gating is "determining the clock on-off based on the data state". Clock gating synthesis can be based on the satisfiability or observability of the signals. It no longer relies on fixed system-level enabling signals. Instead, it dynamically generates gating signals by monitoring the data activities within the functional modules, such as whether the trigger needs to

DOI: 10.54254/2755-2721/2025.GL30920

update its state or whether the data is in a stable invalid state. When there is no effective change in the data within the module (such as clock switching being a redundant activity), the gating signal blocks the clock; when data needs to be transmitted or processed, the clock operates normally, fundamentally reducing invalid clock pulses. Clock gating synthesis can be based on the satisfiability or observability of the signals. Therefore, the satisfiability clock gating condition depends on the circuit behavior that occurs from the past to the current clock cycle [10].

3.5. Data driven based clock gating

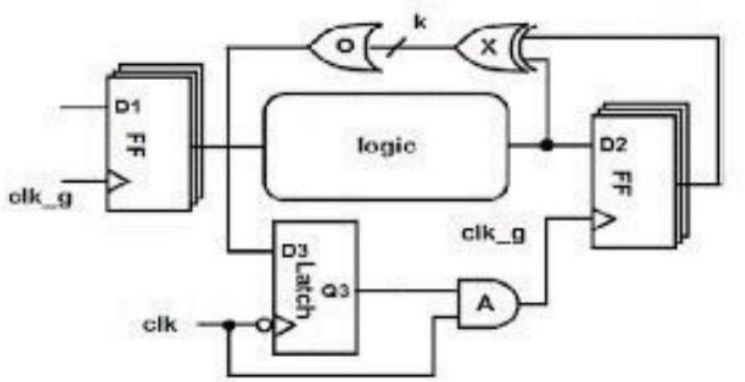

Figure 7. Data driven based clock gating [7]

Figure 7 above is a data-driven clock gating technology. One drawback of data-driven gating is that its time window is short and it is sensitive to delay. "XOR" (exclusive OR operation), "OR", latches, and "AND" gates have overall delays, and this delay must be strictly less than the setup time of the flip-flop; otherwise, it will lead to timing violations. Another drawback is that the risk of critical path expansion increases. As the length of the circuit's critical path increases, the delay percentage of the gating unit will rise. Suppose that by reducing the size or gradually raising the transistors of the non-critical path to a high threshold voltage (HVT) to further save power, a critical situation will occur, and the delay will be elongated. Compared with other gating technologies, the design method of data-driven gating is more complex. To minimize power consumption, the flip-flops should be combined together to make their flip-flop characteristics highly correlated [7].

3.6. Autogated clock gating

The core circuit for implementing the Lightweight Attention Mechanism-Convolutional-Gated Recurrent Unit technique is the Auto Gated Flip flop, illustrated in Figure 8. When the clock signal reaches its falling edge, the main latch of the auto-gated flip flop turns transparent. At this stage, the output must stay stable, with the stable duration exceeding the setup time prior to the clock’s rising edge. In contrast, when the main latch is in a non-transparent state, the XOR gate determines the slave latch’s behavior—either switching its state or retaining the current one. If the slave latch retains its original configuration, the clock pulse will be blocked or let through accordingly.

DOI: 10.54254/2755-2721/2025.GL30920

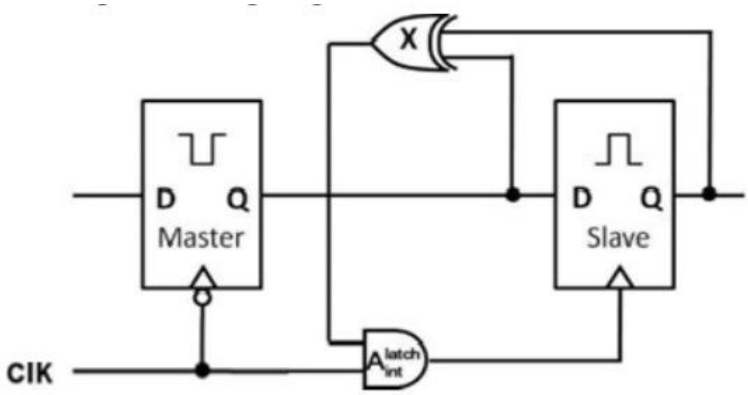

Figure 8. Autogated clock gating [7]

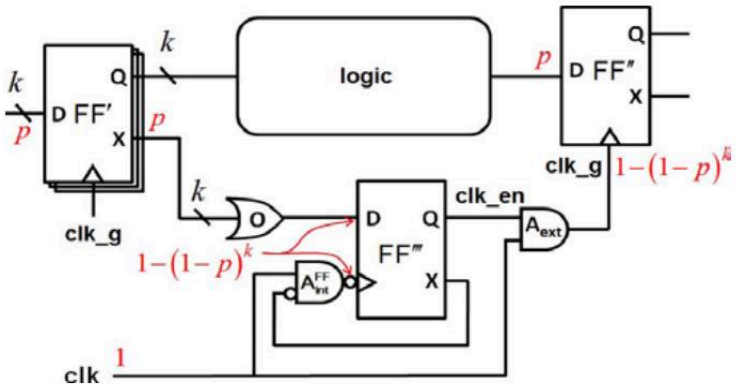

Figure 9. Look-ahead based clock gating [11]

3.7. Look-ahead based clock gating

Look-ahead clock gating(Figure 9) does not rely on real-time data from the current cycle; instead, it uses the clock enable signal from the previous cycle of each flip-flop to control the on-off of the clock in the current cycle. This "forward" design gives the gating signal more time to stabilize, further reducing redundant switching, achieving more thorough power consumption optimization, and fundamentally alleviating timing pressure. LACG has enabled the rapid development of AGFF, achieving three goals: stopping the clock pulse in the main latch as well, further reducing redundant switching, and achieving more thorough power consumption optimization. Secondly, it makes it applicable to large and general designs, capable of flexibly being applied to complex large-scale digital circuits, with better compatibility than data-driven and other dedicated gating technologies. Thirdly, it avoids strict timing constraints and eliminates the demanding requirement in data-driven gating that "the gating unit delay must be less than the trigger setup time" [12].

DOI: 10.54254/2755-2721/2025.GL30920

3.8. Comparison of clock gating techniques

Table 1. Comparison of different clock gating techniques [7]

Latch based CG	Gate based CG	FF based CG	
avoid glitches	gliches affect	gliches affect	
Long sleep period	avoid sleep period	avoid sleep period	
Low dynamic power	high dynamic power	high dynamic power	
Less switching activity	High switching activity	High switching activity	
Good performance	moderate performance	bad performance	
occupy small area	occupy small area	occupy large area	
Synthesis based CG	Auto-gated CG	Data driven based CG	Look ahead based CG
more power	more power	less power	less power
high redundant problem	less redundant problem	avoid redundant problem	avoid redundant problem
easy implementation	easy implementration	difficult implementration	easy implementration
less timing constraint	high timing constraint	moderate timing constraint	less timing constraint

From the table 1 data, Latch-based CG performs better in terms of dynamic power consumption, switching activity, performance and area, and can avoid glitches and have a longer sleep cycle. Data-driven based CG and Look-ahead based CG can effectively avoid redundancy issues and reduce power consumption, but the data-driven implementation is more difficult.

Overall comparison shows that the effective method for reducing dynamic power consumption can be prioritized as Latch-based CG, as its low dynamic power consumption and low switching activity characteristics are clearly superior. If redundancy issues need to be avoided, Look-ahead based CG is the better choice, as it is easier to implement and has loose timing constraints, while also effectively reducing clock switching power.

4. Application: clock gating techniques in Central Processing Units (CPUs)

The extensive power consumption of CPU in modern devices is a burning issue. Advanced digital components inevitably leads to higher power consumption. With the implementation of clock gating technology, an effective limitation of dynamic power consumption and heat generation may be achieved. For instance, Intel's (a known technology company) high-performance CPUs use fine-grained and coarse-grained clock gating to optimize power efficiency without the sacrifice of performance. Despite its effectiveness, there is still some flaws. When a clock is gated, the circuit enters a low-power state, but re-enabling it requires time. The time delay is crucial because it impacts performance and even power efficiency (if wake-up latency is too long).

$$P_{dynamic} = \alpha \times C \times V^2 \times f \qquad \alpha : \text{activity factor } (0 \text{ to } 1) \tag{1}$$

5. Conclusion

This study aimed to review how clock gating technology benefits in dynamic power optimization in CMOS integrated circuits. Furthermore, this paper provides an analysis of the different types of clock gating techniques, estimation of dynamic power consumption based on simulation, and real-life applications such as clock gating in CPUs. According to data, there is a significant amount of

DOI: 10.54254/2755-2721/2025.GL30920

dynamic power reduction after using clock gating technology (around 20% reduction) in ISCAS'89 benchmark circuits. To take note, this paper mainly discusses a generalized overview of clock gating techniques in CMOS, where each subtopic offers a unique perspective, instead of an in-depth discussion of a specific area.

Despite uncertainties in this paper, it still covers the research gap of dynamic power optimization in CMOS: with clock gating technology. Since CMOS and clock gating are both extensively utilized in digital areas, this paper addresses the importance of dynamic power consumption and proposes solutions to optimize it.

Author contribution

Yutong Cai, Youruo Hu, and ChangJui Liu contributed equally to this work and should be considered co-first authors.

References

[1] Y. Hu, J. L. Solere, D. Lachartre and R. Tutchetta, "Design and performance of a low-noise, low-power consumption CMOS charge amplifier for capacitive detectors, " in IEEE Transactions on Nuclear Science, vol. 45, no. 1, pp. 119-123, Feb. 1998, doi: 10.1109/23.659562.

[2] B. T. Geetha, B. Padmavathi and V. Perumal, "Design methodologies and circuit optimization techniques for low power CMOS VLSI design, " 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), Chennai, India, 2017, pp. 1759-1763, doi: 10.1109/ICPCSI.2017.8392016.

[3] E. Macii, L. Bolzani, A. Calimera, A. Macii and M. Poncino, "Integrating Clock Gating and Power Gating for Combined Dynamic and Leakage Power Optimization in Digital CMOS Circuits, " 2008 11th EUROMICRO Conference on Digital System Design Architectures, Methods and Tools, Parma, Italy, 2008, pp. 298-303, doi: 10.1109/DSD.2008.90.

[4] L. Benini, "Leading edge low power design [SoCs], " Proceedings of the ASP-DAC Asia and South Pacific Design Automation Conference, 2003., Kitakyushu, Japan, 2003, pp. 385-389, doi: 10.1109/ASPDAC.2003.1195045.

[5] Hu, Kunpeng & Hou, Xingyu & Lin, Zicheng. (2024). Advancements In Low-Power Technologies: Clock-Gated Circuits and Beyond. Highlights in Science, Engineering and Technology. 81. 218-225. 10.54097/qed5f182.

[6] J. Yan. (2012). Research on Estimation Methods and Optimization Strategies for Seed Gate-Level Power Consumption (Master's Thesis, Anhui University). Master's Degree

[7] T. Chindhu S. and N. Shanmugasundaram, "Clock Gating Techniques: An Overview, " 2018 Conference on Emerging Devices and Smart Systems (ICEDSS), Tiruchengode, India, 2018, pp. 217-221, doi: 10.1109/ICEDSS.2018.8544281.

[8] Srinivasan, N., Prakash, N. S., & Sundari, B. B. T. (2015). Power reduction by clock gating technique. Procedia Technology, 21, 631-635.

[9] Figueroa Álvarez, J. (2012). Clock gatting for latch based design.

[10] Y. -Y. Dai and R. K. Brayton, "Verification and Synthesis of Clock-Gated Circuits, " in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 2, pp. 366-379, Feb. 2019, doi: 10.1109/TCAD.2018.2808231.

[11] Murlidharan, V., Vignesh, M., & Varatharaj, M. (2014). Clock gating based on auto-gated flip-flops. IEEE Transactions on Circuits and Systems I: Regular Papers, 61(5), 1465-72.

[12] Chi-Ying Tsui, Massoud Pedram, and Alvin M. Despain. 1993. Efficient estimation of dynamic power consumption under a real delay model. In Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design (ICCAD '93). IEEE Computer Society Press, Washington, DC, USA, 224–228.