Proceedings of CONF-MSS 2026 Symposium: Mechanical Control and Automation
DOI: 10.54254/2755-2721/2026.BJ31412

Research on the Influence of Transistor Electronic Characteristics on the Electromagnetic Compatibility of Integrated Circuits and the Countermeasures

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Abstract. Focusing on the electronic characteristics of transistors, this paper examines their impact on the electromagnetic compatibility (EMC) of integrated circuits and explores optimization strategies. Firstly, the specific mechanism of transistors in relation to electromagnetic interference (EMI) is revealed by analyzing the switching characteristics and noise characteristics of transistors. At the same time, the influence of transistor characteristics on the signal integrity and anti-interference ability of integrated circuits is evaluated. Then, in the design of regulated power supplies and PID controllers, technical schemes are proposed that meet EMC requirements, including filtering, shielding, and anti-interference algorithms. The interaction between these measures and transistor characteristics is also discussed. It is noted that optimizing transistor parameters and designing circuits properly can significantly enhance the EMC performance of the system. Finally, the relevant achievements are summarized, and the direction for further exploring the combination of transistor characteristics and new EMC technologies in the future is outlined. This paper provides practical guidance for improving the reliability of integrated circuits.

Keywords: transistor electronic characteristics, electromagnetic compatibility, electromagnetic interference, regulated power supply, PID controller

1. Introduction

With the rapid advancement of modern electronic technology, integrated circuits (ICs) have become the core backbone of the intelligent society, widely applied in communications, medical devices, automotive electronics, and industrial control systems. 5G communication systems rely on high-density radio frequency ICs to process millimeter-wave signals, demanding transistors with ultra-high-speed switching capabilities, while implantable medical devices use nanoscale transistors to control leakage current and power consumption precisely. However, in complex electromagnetic environments, the interaction between transistor electronic characteristics and electromagnetic compatibility (EMC) has become a critical factor restricting IC reliability. The nonlinear characteristics of transistors, such as random telegraph noise from gate oxide tunneling effects and

DOI: 10.54254/2755-2721/2026.BJ31412

threshold voltage drift caused by hot carrier injection, trigger electromagnetic interference (EMI) and degrade power supply integrity, posing significant challenges for EMC design.

Existing research has primarily focused on EMC optimization at the circuit and system levels; however, there is a lack of in-depth analysis of the intrinsic correlation between transistor microscopic electronic characteristics (e.g., switching speed, noise performance) and system-level EMC performance. As electronic systems face increasingly complex electromagnetic environments —such as interference between on-board radar and power battery management systems in intelligent driving—clarifying this mapping relationship has become an urgent need to improve the reliability of high-density ICs. EMC is not only crucial for ICs to maintain functionality in harsh environments but also a key threshold for market access, as products failing to meet standards like IEC 61000-4 face prohibitions or recalls, causing substantial economic losses.

This review seeks to thoroughly elucidate the method by which transistor electronic properties influence IC EMC, underscore the need of focused optimization, and furnish practical technical references for augmenting IC reliability and market competitiveness.

2. Principles of electromagnetic compatibility of integrated circuits

2.1. Definition of electromagnetic compatibility

Electromagnetic Compatibility (EMC) is the most important feature of an electronic device or system. It means that the device or system can keep working as it should in an electromagnetic environment without being impacted by electromagnetic phenomena from itself or from outside sources. It has two main parts: electromagnetic immunity and electromagnetic interference (EMI) suppression. The first one mandates that the noise made by the device during use, whether it is conducted or radiated, meets international requirements. For example, the CISPR 22 standard sets limitations on radiation disturbance for information technology equipment (40 dBμV/m in the 30 MHz-1 GHz spectrum). The latter refers to the device's ability to maintain functional integrity under external interference, which must meet the test levels specified in the IEC 61000-4 series, including IEC 61000-4-2 (Electrostatic Discharge Immunity) and IEC 61000-4-3 (Radiated, Radio-Frequency Electromagnetic Field Immunity) [1]. The dependable functioning of electronic systems in complex electromagnetic settings is based on these two factors.

With the increasing integration and operating frequency of electronic equipment, EMC has become a bottleneck restricting the development of modern technology, and its importance is clearly reflected in various fields. In the medical field, the switching of gradient coils in Magnetic Resonance Imaging (MRI) systems can generate intense transient electromagnetic fields with peak values up to tens of kV/m. If supporting monitoring equipment fails to pass the Level 3 immunity test specified in IEC 61000-4-3 (10 V/m field strength in the 80 MHz-1 GHz band), it may result in distorted heart rate monitoring data, potentially endangering patient safety [2]. In the automotive electronics field, conducted interference generated by the operation of on-board inverters in new energy vehicles, if not compliant with the requirements of the ISO 11452-2 standard, may cause false triggering of on-board radar and affect the decision-making of autonomous driving systems. In industrial scenarios, harmonic interference generated by the operation of frequency converters, if exceeding the limits specified in the IEC 61000-3-2 standard, can result in delayed execution of PLC controller commands and cause production line shutdowns.

From an economic and market perspective, EMC is a "pass" for products to enter the market. Electronic products that fail to obtain CE-EMC certification are prohibited from entering the European market. In 2023, 32% of electronic product recall cases reported through the EU RAPEX

DOI: 10.54254/2755-2721/2026.BJ31412

system were due to non-compliant EMC, with an average recall loss of over 5 million euros per case [3]. Therefore, integrating EMC characteristics into chip-level design is crucial. For example, reducing switching noise by optimizing transistor channel doping lays the foundation for system-level electromagnetic compatibility.

2.2. Electromagnetic interference and immunity

The two main components of electromagnetic compatibility are electromagnetic susceptibility (EMS) and electromagnetic interference (EMI). EMI, which is separated into conducted interference and radiated interference, is the term used to describe the unintentional reaction of an electronic system brought on by either internal or external electromagnetic energy. High-frequency switching power supplies frequently experience conducted interference. For example, current spikes in the 150 kHz–30 MHz band produced by server power modules can travel through power lines to the power grid, impacting the stability of nearby equipment's power supply. The transient electromagnetic waves in the 2.4 GHz and 5 GHz bands produced by the fast switching of transistors in smartphone RF chips are a common example of radiated interference. Without suppression, these waves can interfere with the signal reception of nearby Bluetooth headsets, causing audio stutters [4]. These interferences manifest as burst noise in the time domain, spanning a frequency range from kHz to GHz, which can compromise the signal integrity of integrated circuits, leading to eye diagram closure and increased bit error rates.

The capacity of the device to continue operating in an electromagnetic environment, including its resistance to interferences such electrostatic discharge and electrical rapid transients, is reflected in EMS. It is closely associated with the IEC 61000-4 series' test levels. Failures brought on by EMC problems are frequent in real-world applications. When frequency converters in the workshop were turned on and off, the servo driver of a particular kind of industrial robot experienced increased tunneling effects in its internal CMOS transistors due to the lack of protection against electrical fast transient interference (IEC 61000-4-4). This resulted in an increase in motor positioning error from ±0.02 mm to ±0.1 mm, which failed to meet the requirements of precision machining [5]. Because it failed the common-mode interference test outlined in IEC 61000-4-6 and the FinFET devices in the navigation signal demodulation chip were impacted by parasitic coupling within their three-dimensional structure, a specific on-board navigation system encountered positioning drift when traveling through high-voltage power lines. After thunderstorms, household routers often disconnect from the network. This is mainly because, according to IEC 61000-4-2, electrostatic discharge damages the gate oxide layer of transistors in the router's RF circuit, causing a significant loss in signal transmission power [6].

Integrated circuits' operating frequency, packaging, and layout design all have a direct impact on how susceptible they are to EMI. Interference may be made worse by tunneling effects in CMOS techniques and the three-dimensional design of FinFET devices [7]. Timing mistakes happen when EMI energy surpasses the logic gate noise margin. System reliability is directly impacted by EMS performance; for instance, the CAN bus in automotive electronics needs a frame error rate of less than 10^{-2} [8]. SPICE models and mixed-signal simulations can be used to quantify electromagnetic radiation and harmonic distortion. Noise can be decreased and the common-mode rejection ratio can be increased by using strategies including deep N-well isolation technology, differential signal design, and transistor intrinsic parameter tuning.

DOI: 10.54254/2755-2721/2026.BJ31412

3. The impact of transistor electronic characteristics on the electromagnetic compatibility of integrated circuits and design guidelines

As the core device of integrated circuits, t anti-interference capability, both of which jointly constitute the core influencing factors of integrated circuit electromagnetic compatibility (EMC). The following analy a perspective and targeted design guidelines.

3.1. EMC action principles of core electronic characteristics

3.1.1. Switching characteristics and EMI generation mechanism

The main sources of EMI excitation during transistor switching are the voltage slew rate (dv/dt) and current slew rate (di/dt). Maxwell's electromagnetic theory states that steep switching edges create high-frequency oscillating electromagnetic fields that connect to nearby circuits via conduction or radiation. For instance, when CMOS transistors switch, the power path's parasitic inductance experiences brief voltage spikes, the magnitude of which is precisely proportional to the current's rate of change, or di/dt. These spikes can enhance the level of transmitted interference by more than 20 dB at switching frequencies higher than 1 GHz [9].

Synchronous switching of multiple transistors exacerbates interference effects. According to the Biot-Savart law, synchronously changing currents in loop antennas form, and the radiated field strength increases nonlinearly with the number of switching transistors. Although FinFET structures optimize switching speed, the parasitic capacitance coupling effect caused by their three-dimensional structure increases radiated interference in the high-frequency band (2-5 GHz) by 15%-25% compared to traditional planar transistors [10].

3.1.2. Interference superposition effect of noise characteristics

Transistors' intrinsic noise affects EMC through two paths: direct coupling and energy amplification. Thermal noise originates from carrier thermal motion and exhibits white noise characteristics. In high-frequency circuits, it superimposes on signal links, reducing the signal-to-noise ratio (SNR). Especially in radio frequency circuits, thermal noise can reduce the conducted interference limit margin by more than 10 dB [11]. Leakage current, as a low-frequency interference source, not only directly generates electromagnetic radiation but also causes a rise in device temperature, further amplifying thermal noise and forming a "noise-temperature rise" positive feedback loop.

Secondary noise sources cannot be ignored. Shot noise is caused by statistical fluctuations in the movement of carriers crossing barriers, which can easily lead to nonlinear distortion in broadband systems. Flicker noise (1/f noise) originates from material interface defects, and its low-frequency-dominant spectral characteristics deteriorate the phase stability of analog circuits, threatening precision control circuits [12].

3.1.3. Physical essence of anti-interference characteristics

A transistor's anti-interference capability essentially refers to its ability to resist disturbances from external electromagnetic energy, which primarily depends on the device's structure and material properties. External electromagnetic interference couples with parameters such as PN junction capacitance and parasitic inductance inside transistors, changing carrier transport characteristics and causing operating point drift or logic false triggering. For example, transient electric fields generated

DOI: 10.54254/2755-2721/2026.BJ31412

by electrostatic discharge can cause tunneling in the gate oxide layer of MOSFETs, permanently changing the threshold voltage and reducing the circuit's anti-interference threshold [13].

Materials and structures determine the basic anti-interference performance. High-mobility materials (e.g., GaN) exhibit fast carrier transport speeds and short response times to external electric field disturbances, with anti-interference performance 30% higher than that of traditional Si materials. Deep N-well isolation structures can reduce signal distortion caused by electromagnetic radiation by 40% by suppressing substrate coupling [14].

3.2. Transistor design guidelines for EMC optimization

Electromagnetic compatibility (EMC) optimization at the transistor level can be achieved through coordinated control of switching behavior, noise suppression, device structure, and packaging. Gradient drive techniques are commonly adopted to moderate switching slopes; by maintaining the current slew rate (di/dt) below 5 A/ns while satisfying response speed requirements, radiated interference can be reduced by 15–20 dB [15]. At the device scale, careful optimization of transistor dimensions and gate oxide thickness helps balance switching speed against parasitic effects. For instance, at the 130 nm process node, limiting the channel length to approximately 0.15 μm mitigates high-frequency interference caused by parasitic capacitance coupling. Electromagnetic interference peaks can be further suppressed by avoiding synchronous switching of multiple transistors through timing staggering within a 10–20 ns window. Noise performance is improved by selecting low-defect-density gate oxides, which reduces 1/f noise by 25–30% [16], and by employing cascode structures with optimized biasing to suppress the Miller effect and thermal noise. For high-temperature applications, wide-bandgap materials such as SiC significantly reduce leakage-induced noise amplification. In addition, flip-chip packaging combined with shielding layers lowers electromagnetic coupling by over 50% [17]. At the same time, RC snubber networks (10–100 Ω, 10–100 pF) enhance transient suppression and enable compliance with IEC 61000-4-2 Level 4 ESD requirements. Finally, optimized channel doping gradients improve reverse recovery stability and reduce parameter drift under electromagnetic pulse exposure.

4. Transistor electronic characteristics and electromagnetic immunity

Transistor electromagnetic immunity refers to the ability to maintain stable electrical performance and functional integrity when exposed to external electromagnetic interference (EMI). The physical mechanisms of interaction between the internal electronic processes of the transistor and external electromagnetic energy determine its core. Below is a detailed analysis of the key physical phenomena, their impacts, and corresponding solutions supported by practical cases.

4.1. Physical phenomena affecting electromagnetic immunity

4.1.1. Carrier transport disturbance induced by electromagnetic fields

External electromagnetic fields (including electrostatic discharge and radiated electromagnetic waves) directly perturb the carrier transport process within transistors. According to the Lorentz force law, charged carriers (electrons/holes) in the channel are subjected to a Lorentz force under the action of external electric and magnetic fields, causing deviations from the normal transport path. For example, in CMOS devices, a transient electric field of 100 V/m can deflect carrier trajectories by more than 20%, resulting in current fluctuations and logic level misjudgments [18].

DOI: 10.54254/2755-2721/2026.BJ31412

The displacement current produced by alternating electric fields in high-frequency electromagnetic settings modifies the transistor's PN junction's depletion layer width, changing the junction capacitance and dynamic resistance. In FinFET devices with three-dimensional architectures, this modulation effect is very noticeable. External high-frequency signals can be coupled by the parasitic capacitance between the fin and the substrate, which can cause threshold voltage drift of up to 50 mV and impact the timing stability of the circuit [19].

4.1.2. Nonlinear effects exacerbating interference susceptibility

Transistor nonlinear characteristics are key factors amplifying electromagnetic interference. When the amplitude of external interference exceeds the linear operating range of the transistor, nonlinear effects such as harmonic generation and intermodulation distortion will occur. For bipolar transistors, the nonlinearity of transconductance (gm) converts external single-frequency interference into multi-frequency harmonic components, which overlap with the useful signal spectrum and degrade the signal-to-noise ratio (SNR) [20].

The secondary breakdown effect of power transistors is a typical nonlinear failure mechanism. Under the combined action of high voltage and strong electromagnetic pulses, the local current density of the transistor increases sharply, resulting in the formation of a hot spot. The positive temperature coefficient of the semiconductor material causes the hot spot resistance to decrease, leading to further current concentration and eventual device burnout. This phenomenon is particularly prominent in Si-based power MOSFETs, with a failure rate increased by 3-5 times under electromagnetic pulse interference [21].

4.1.3. Noise source coupling and amplification

Transistor intrinsic noise and external interference form a coupling amplification effect, worsening immunity. Thermal noise, which is proportional to the square root of temperature and bandwidth, will be superimposed with external conducted interference, making weak signal detection circuits more susceptible to false triggering. For example, in the analog front-end of industrial sensors, the thermal noise of the input transistor and the electromagnetic interference from the power line are coupled through the substrate, resulting in a measurement error increase of more than 15% [22].

1/f noise (flicker noise) originating from interface defects is more sensitive to low-frequency electromagnetic interference. External low-frequency interference (such as 50 Hz power frequency noise) can modulate the 1/f noise spectrum, thereby extending the noise's influence into the signal frequency band. In precision PID controllers, this coupling effect can cause the control signal to jitter, reducing the stability of the control system [23].

4.2. Key nonlinearities, noise sources, and their circuit-level EMC impacts

Two of the main risk factors for electromagnetic compatibility (EMC) degradation at the circuit level are transistor nonlinearity and intrinsic noise sources. Under multi-frequency excitation, intermodulation distortion results from a transistor's gain changing with input voltage due to transconductance nonlinearity. This phenomenon can cause adjacent channel interference in radio-frequency integrated circuits and cause them to fall short of the CISPR 22 adjacent channel leakage ratio standards [24]. Similar to this, MOSFETs' output conductance nonlinearity rises with drain-source voltage, increasing the susceptibility of output signals to external interference modulation and raising voltage ripple in power management circuits by two to three times, which jeopardizes

DOI: 10.54254/2755-2721/2026.BJ31412

downstream circuit stability [25]. In addition, parasitic capacitances and inductances exhibit frequency-dependent nonlinear behavior; under high-frequency electromagnetic interference, gate–drain capacitance (Cgd) can induce Miller-effect amplification, significantly increasing interference susceptibility [26]. Noise mechanisms further exacerbate EMC issues: thermal noise, originating from carrier thermal motion, couples directly into the signal path and can degrade the noise figure of low-noise amplifiers by more than 3 dB [27], while shot noise in bipolar and wide-bandgap devices increases phase noise in GaN HEMT power amplifiers, adversely affecting bit error rates [28]. At elevated temperatures, leakage current noise—including subthreshold and gate-oxide tunneling components—rises exponentially and may cause quiescent current fluctuations exceeding 20%, triggering false protection events in automotive electronic systems [29].

4.3. Device- and circuit-level EMC enhancement strategies

Coordinated optimization at the device, circuit, and system levels is necessary to improve integrated circuits' electromagnetic compatibility (EMC). Adoption of sophisticated architectures and wide-bandgap materials is crucial at the device level. GaN and SiC devices have low parasitic characteristics and high breakdown voltage; GaN high-electron-mobility transistors (HEMTs) can reduce threshold voltage drift caused by electromagnetic interference by about 60% when compared to traditional Si transistors [30]. A high-mobility two-dimensional electron gas (2DEG) is further formed by the AlGaN/GaN heterojunction, allowing for quick recovery from carrier disruptions brought on by external electromagnetic fields. Optimization at the process level is equally crucial. Retrograde channel doping improves immunity by up to 40% in CMOS technology by suppressing threshold voltage shifts under electromagnetic pulse exposure and increasing resistance to hot-carrier injection [31].

Packaging and isolation techniques significantly influence EMC performance. Flip-chip packaging reduces parasitic inductance by nearly 50% compared with wire bonding, thereby weakening electromagnetic field coupling, while deep N-well isolation suppresses substrate-coupled noise by approximately 35% [32]. At the circuit level, RC buffer networks connected at the transistor gate effectively absorb transient interference energy and suppress voltage overshoot; in automotive IGBT drive circuits, this approach reduces EMI-induced turn-on delay fluctuations from 20 ns to 5 ns [33]. In order to comply with IEC 61000-4-2 Level 4 criteria, transient voltage suppressor (TVS) diodes further improve electrostatic discharge robustness. In industrial sensor applications, differential amplification and negative feedback enhance common-mode rejection, resulting in CMRR values above 80 dB and a 70% reduction in interference-induced signal distortion [34]. Lastly, radiation coupling and ground-loop interference are successfully reduced by optimized PCB architecture and grounding techniques, such as differential routing, low-impedance star grounding, and maintaining sufficient space [35]. Significant increases in EMC compliance, reliability, and measurement accuracy have been demonstrated by these integrated techniques, which have been validated across automotive ECUs, industrial PLCs, and medical monitoring systems [36-38].

5. EMC-optimized design schemes for core components

As critical components of integrated circuits, regulated power supplies and PID controllers directly determine the overall reliability of the system through their EMC performance. The following integrates the core design strategies of these two components, analyzes their correlation with transistor characteristics, and clarifies the application scenarios and practical value of each scheme.

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5.1. Core anti-interference design at the hardware level

5.1.1. Synergistic application of filtering and shielding technologies

Filtering technology blocks interference propagation through spectrum suppression, while shielding technology reduces field coupling through physical isolation, forming the foundation of hardware anti-interference. The π-type filter network, combined with X capacitors and common-mode inductors, can suppress both common-mode and differential-mode noise simultaneously. It is suitable for high-interference scenarios such as power supply input terminals, reducing conducted interference in the 150 kHz-30 MHz band by more than 60% [39]. The LC low-pass filter is adapted for output current ripple suppression; in precision instrument power supply circuits, it can control the voltage spike amplitude within 5%.

Shielding technology requires the selection of materials and structures based on specific application scenarios. High-frequency switching power supply modules, for instance, adopt fully enclosed metal shields with silver-plated copper to effectively absorb radiated energy in the 2-5 GHz band, making them suitable for high-frequency equipment such as communication base stations and radars [40]. Nickel-based alloy shielding layers are used in high-temperature environments (e.g., automotive engine compartments) to balance electromagnetic performance and heat resistance. In layout design, the distance between strong interference sources and sensitive circuits should exceed 5 mm, and power loop layout optimization can reduce the di/dt path area to suppress magnetic field coupling.

5.1.2. Transistor characteristic adaptation and circuit optimization

Hardware design must closely match the inherent characteristics of transistors: for SiC/GaN wide-bandgap transistors, their high-speed switching characteristics generate high-frequency harmonics. The filter cutoff frequency needs to be increased to more than 5 times the switching frequency, and RC snubber networks (R=10-100 Ω, C=10-100 pF) are used to suppress transient interference caused by dv/dt [41]. Bipolar transistors are prone to secondary breakdown; in high-power circuits, current limiting protection and thermal design must be combined to avoid radiation spectrum expansion due to thermal runaway.

The selection of the package and isolation technology directly affects the anti-interference effects. Flip-chip packaging can reduce parasitic inductance by 50%, making it suitable for high-frequency power conversion scenarios. Deep N-well isolation technology suppresses substrate-coupled noise, reducing signal distortion by 40% in mixed-signal circuits [42]. Optocoupler isolation technology is suitable for mixed strong and weak current scenarios, such as signal interfaces of industrial PLC controllers, completely cutting off electrical coupling paths.

5.2. Anti-interference optimization strategies for software algorithms

Software algorithms compensate for the limitations of hardware design by utilizing signal processing and parameter adjustments. The moving average filtering algorithm is simple to implement. It has low resource consumption, making it suitable for low-speed sampling scenarios (e.g., temperature and pressure sensor signal processing), which reduces the random noise amplitude by 30%-50%. Kalman filtering achieves accurate estimation based on dynamic noise models, adapting to high-speed dynamic systems (e.g., industrial robotic arm servo control) and maintaining signal-to-noise ratio under electromagnetic interference [43].

DOI: 10.54254/2755-2721/2026.BJ31412

Adaptive anti-interference algorithms target complex and variable electromagnetic environments. Adaptive notch filters can real-time track periodic interference, such as 50 Hz power frequency noise and inverter harmonics, making them suitable for industrial scenarios with frequent power grid fluctuations. The compensation algorithm based on disturbance observers (DOB) can reconstruct the equivalent electromagnetic interference model; in autonomous driving, it can reduce positioning errors from ±0.1 mm to ±0.02 mm [44]. Fuzzy PID or neural network online parameter tuning strategies dynamically compensate for performance degradation caused by transistor parameter drift, thereby adapting to the operation of outdoor electronic equipment over extended periods. In digitally controlled power supplies, adding anti-aliasing filters in the feedback loop avoids switching frequency modulation caused by sampling noise, adapting to precision electronic equipment with strict power supply stability requirements [45].

5.3. Design scheme selection and application value in different scenarios

EMC-optimized design schemes must be tailored to specific application environments. In high-frequency and high-speed systems such as 5G base-station power supplies and millimeter-wave radar control circuits, the combined use of SiC/GaN transistors, π-type filter networks, and flip-chip packaging, together with adaptive Kalman filtering algorithms, effectively reduces EMI source intensity and suppresses high-frequency interference propagation, ensuring signal integrity above 1 GHz under low-latency requirements [46]. In high-temperature and harsh environments, including automotive electronics, industrial inverters, and aerospace systems, nickel-based shielding layers and wide-bandgap devices complemented by fuzzy PID tuning improve robustness against thermal parameter drift, raising EMC compliance rates to over 95% across −40 °C to 125 °C [47]. For precision-control applications such as medical monitoring and laboratory instruments, LC filtering, deep N-well isolation, and moving-average algorithms suppress weak-signal interference, enhancing control accuracy by 40% and limiting measurement errors to within ±0.1% [48].

6. Conclusion

This study systematically investigates the mechanism by which transistor electronic characteristics influence the electromagnetic compatibility (EMC) of integrated circuits and proposes targeted optimization strategies. Experimental and simulation results confirm that transistor switching characteristics (di/dt, dv/dt) and noise characteristics (thermal noise, leakage current, 1/f noise) are key factors determining the intensity of electromagnetic interference (EMI) and the system's anti-interference capability. For instance, steep switching edges induce high-frequency radiation, while interface defect-induced 1/f noise degrades the stability of low-frequency signals [49]. Wide-bandgap materials (e.g., SiC/GaN) and advanced structures (FinFET) can reduce switching losses by over 40% and suppress intrinsic noise, significantly improving EMC performance [50].

The integrated optimization schemes proposed in this paper—covering device selection, circuit design, and software algorithms—have practical application value. Hardware-level measures such as π-type filtering, metal shielding, and deep N-well isolation, combined with software algorithms like adaptive Kalman filtering and fuzzy PID tuning, form a multi-dimensional EMC protection system. These schemes have been verified to reduce conducted interference by 30%-50% and enhance system immunity to electromagnetic pulses, meeting international standards such as IEC 61000-4 [51].

Limitations of this research include the insufficient dynamic range of the test platform for high-frequency (above 5 GHz) electromagnetic environments and the lack of in-depth analysis of cross-

DOI: 10.54254/2755-2721/2026.BJ31412

scale coupling mechanisms between transistor thermal effects and electromagnetic radiation. Future work will focus on developing wide-frequency-domain test systems and multi-physics coupling simulation tools, exploring EMC design for emerging devices (e.g., GaN HEMTs) in 5G and automotive electronics, and establishing a chip-package co-design evaluation system to promote the integration of semiconductor technology and electromagnetic protection innovation.

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DOI: 10.54254/2755-2721/2026.BJ31412

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