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Research on Collaborative Optimisation of High-power Chip Multi-dimensional Thermal Management Technology and Integrated Devices

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Abstract. In response to the thermal management bottlenecks brought about by the high integration and high powerization of high-power chips, as well as the performance compatibility problems of on-chip integrated interconnection and energy storage devices, this paper carries out multi-structure coupled thermal management, network-on-chip (NoC) architecture fault tolerance optimisation, on-chip energy storage device material modification and high-performance thermal interface. Through numerical simulation and experimental verification, the performance laws of bionic microchannels jet shock-coupled heat dissipation, gradient porous-heat pipe composite heat dissipation, topology optimisation-microchannel integrated liquid cooling, and dry ice particle jet phase change heat dissipation are revealed; a machine learning-driven NoC fault tolerance core mapping model is built, and the packaging is supplemented with the channel shortening and equalisation technology of the line NoC. The research results show that the bionic coupled heat dissipation system can reduce the maximum temperature of the 800W chip by 8.47%, the topology optimisation microchannel integrated liquid cooling structure achieves 4.28K cooling, the dry ice jet system realises the safe temperature control of the chip at 300W/cm² heat flow density, and the liquid metal TIM at 90W Compared with the traditional hot silicone grease, the temperature is 9.8℃, and the RI-CSF scheme of wireless NoC achieves a significant SINR improvement, and the capacity of integrated energy storage devices is increased to 34.2 mF/cm². This research provides technical support for the collaborative design of high-efficiency thermal management and integrated devices of high-power chips.

Keywords: high-power chip, thermal management, network-on-Chip, thermal interface material, topology optimization

1. Introduction

1.1. Research background and significance

With the rapid development of artificial intelligence, quantum computing and other technologies, the chip has evolved towards high integration and high-power density. Its heat current density has exceeded 100 W/cm², and the power of some special chips exceeds 700 W [1]. Excessive working

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temperature will lead to chip performance attenuation, shortening of life, and even failure, while the heat dissipation limit of traditional air-cooling technology is only 50 W/cm² [2], which can no longer meet the heat dissipation needs of high-power chips. At the same time, in data centers, the energy efficiency of the cooling system is an important factor, especially in large data centers, where the cooling demand plays a crucial role in the overall energy use efficiency [3], and improving the heat dissipation efficiency is crucial to reducing the overall energy consumption.

In high-power chip applications, with the continuous improvement of chip power and computing demand, the heat of the device has increased significantly, making it difficult for the traditional radiator design and single heat dissipation method to meet the temperature control requirements [4]; with the continuous improvement of device miniatlization and component density, the failure risk of the processor/core in multi-core chips increases, so that the surface The fault-tolerant design of NoC has become the key to ensuring the reliability of the system [5]. In addition, under the constraints of CMOS-compatible materials and post-processing processes, the reliable integration and stability of ReRAM on the chip still face challenges; for example, the W electrode is prone to oxidation and forms an oxidation layer at the W/HfO_2 interface, which significantly affects the stability and reliability of the device switch, which needs to be passed through. Surface/material engineering should be improved [6,7]. Therefore, carrying out collaborative optimization research on multi-dimensional thermal management and integrated devices of high-power chips has important engineering value and academic significance for improving the energy efficiency and reliability of chips.

1.2. Current situation of research at home and abroad

1.2.1. High-power chip thermal management technology

In the field of liquid cooling and heat dissipation, a lotus leaf vein microchannel-jut shock coupling system with a diversion channel is proposed to cool the 800 W chip with mineral oil as a coolant; compared with the basic bionic structure, the circular diversion channel scheme can reduce the maximum temperature of the chip by 8.47% [1]; in addition, some studies have proposed that liquid-cooled radiators with topological optimization and straight microchannels aim to balance thermal performance and hydraulic efficiency. Compared with the traditional straight microchannel, the integrated structure can effectively reduce the temperature and pressure drop [8]. In terms of porous structure heat dissipation, the research on the liquid-cooled heat dissipation structure of integrated topology optimization and microchannel design shows that compared with the traditional straight microchannel design, the maximum chip temperature of this structure is reduced by 4.28 K, and the voltage drop is reduced by 319.42 Pa [9]. In the field of phase change heat dissipation, the study of the closed-loop dry ice particle jet cooling system shows that the optimal intermediate pressure of the DSCR1 system of the built-in air cooler outlet heat exchanger is 0.9 MPa, COP reaches 1.231, and the chip surface can maintain a safe temperature when the dry ice volume fraction is ≥25%, and the diffusion angle is 4°. The unified COP increased by 7.8% [10]. In the field of thermal interface materials (TIM), liquid metal, as a new TIM material, has a significant improvement in thermal conductivity. Research shows that liquid metal TIM shows lower thermal resistance and higher thermal conductivity than traditional thermal silicone grease in terms of improving heat dissipation performance, which significantly improves the thermal management effect [3].

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1.2.2. Chip integrated interconnection and energy storage devices

For the chip-to-chip concurrent wireless link in the package, the proposed covariance regularization and interference perception channel shortening filter (RI-CSF) reception scheme aims to maximize the SINR of the judgment sampling point, while suppressing the ISI and multi-link interference caused by multipaths. To achieve higher SINR and lower BER transmission performance under different concurrency and transmission power conditions [11], for the wireless NoC in the package, the interference-aware channel shortening filter (RI-CSF) scheme can significantly improve the SINR of concurrent transmission and reduce BER, without the need for transmitter coordination [11]. The W electrode oxidation of ReRAM is inhibited by the Al2O3 interface layer, which significantly improves the stability of resistance [7].

1.2.3. Insufficient existing research

The existing dry ice particle jet phase change cooling research is still mainly based on open systems, and the CO2 gas generated by dry ice sublimation is usually not recycled; the relevant work mostly focuses on the sublimation cooling process or nozzle structure design, and dry ice for high thermal flow density chips (such as 300 W/cm²) has not been formed. Generation-ejection cooling-CO2 recycling integrated closed-loop application system, closed-loop circulation and recycling still need to be strengthened [10]; the realization of on-chip device integration under CMOS-compatible material conditions still faces challenges in reliability and stability, and it is necessary to improve device stability and performance through interface/material optimization [6,7].

1.3. Research content and innovation points

This paper focuses on high-power chip multi-structure coupling thermal management, NoC architecture multi-dimensional optimization, integrated energy storage device modification and TIM performance improvement. The technical route is "numerical simulation—experimental verification —performance optimization". The innovative points are as follows: First, propose a multi-structure coupled heat dissipation scheme, covering bionic microchannel-gent, topological microchannel integration, dry ice jet phase change and other technologies; Second, build a machine learning-driven NoC fault-tolerant-low-power collaborative model to supplement wireless NoC channel shortening and balancing technology; Third, realize integrated energy storage CMOS compatibility modification of the device; Fourth, verify the high-efficiency heat dissipation characteristics of gallium-based liquid metal TIM.

2. High-power chip multi-structure coupling thermal management technology

2.1. Leaf vein microchannel-jet shock coupling heat dissipation system

2.1.1. Structural design and simulation model

Based on the lotus leaf vein network structure, the leaf vein microchannel-jet impact system (DLJ-MCHS) with the distribution channel is designed. The distribution channel is set to three configurations: round, quadrilateral and octagonal. The height of the microchannel is 10-34 mm, and the spacing-width ratio of the distribution channel is α=1.0-4.5 [1]. Adopt the standard k-ε turbulence model to set boundary conditions: the coolant is mineral oil (density 804 kg/m³, thermal

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conductivity 0.145 W/m·K), the chip heating power is 800 W, and the inlet temperature is 35℃. After grid independence verification, the grid number is determined to be 4.4 million.

2.1.2. Analysis of simulation results

The comprehensive performance of the circular distribution channel is the best. Compared with the basic bionic structure, the maximum temperature of the chip is reduced by 8.47%, the thermal resistance is reduced by 14.24%, the temperature difference is reduced by 20.50%, and the pressure drop change is extremely small [1]. The optimization law of the height of the microchannel and the spacing of the distribution channel shows that when α=2.0, the heat dissipation performance and lightness are balanced. After the height of the microchannel is 20 mm, the heat dissipation gain that continues to increase is less than 0.05℃ [1].

2.2. Topology optimization - microchannel integrated liquid cooling radiator

2.2.1. Multi-objective optimization design

Based on engineering factors such as heat dissipation performance, processing feasibility/cost and structural strength, the distribution channel spacing-width ratio α=2.0 is preferred; when the height of the microchannel is increased to 20 mm, the improvement of the highest chip temperature is less than 0.05 ℃ (the average temperature improvement is less than 0.10 ℃) [9].

2.2.2. Performance verification compared with thermally conductive silicone grease

Ga75In25 liquid metal TIM can significantly reduce the temperature of the heat source; at 90 W heating power, the temperature of the heat source can be reduced by 9.8 ℃. The experiment matches the numerical simulation results well. The numerical simulation can be used to evaluate the impact of heating power, TIM thickness and interface area on the temperature distribution and heat dissipation performance of the heat source, and use the near-linear relationship between temperature and power for rapid estimation [8].

2.3. Dry ice particle jet closed-loop cooling system

2.3.1. System configuration and thermodynamic model

Design two closed-loop systems, DSCR1 (air cooler outlet built-in heat exchanger) and DSCR2 (intermediate cooler outlet built-in heat exchanger), based on the cross-critical CO2 two-level compression cycle, combined with the Joule-Thomson effect to realize dry ice particle generation [10]. Set the heat flow density of the chip to 300 W/cm² and the cooling capacity to 1 kW, use ASPEN HYSYS to establish a thermodynamic model, and analyze the impact of intermediate pressure and air cooler outlet parameters on the system COP.

2.3.2. Analysis of heat dissipation performance

The performance of the DSCR1 system is better than that of DSCR2. When the outlet pressure of the air cooler is 8.5 MPa and the temperature is 35 ℃, the optimal intermediate pressure is 0.9 MPa, and the COP reaches 1.231 [10]; when the volume fraction of dry ice at the entrance of the radiator is ≥25%, the whole surface of the chip is lower than the 350 K safe temperature; when the diffusion

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angle is 4°, the optimal intermediate pressure of the system rises to 1.032 MPa, and the COP is increased by 7.8% [10].

2.4. Gradient TPMS - heat pipe composite heat dissipation structure

2.4.1. Topological design and preparation

With the cold plate as the design domain, the topological channel is obtained by variable density topology optimization (Darcy interpolation and Helmholtz filter/projection stability geometry), and on this basis, the straight microchannel is embedded to form a topologically optimized microchannel-integrated cold plate; the three-dimensional model uses an aluminum cold plate and water cooling in numerical simulation. The agent is a material system, and a certain thickness of TIM is set between the chip and the cold plate; at the same time, it is pointed out in the article that advanced metal additive manufacturing (such as metal laser powder bed melting) makes this kind of complex structure feasible for processing [9].

2.4.2. Verification of heat dissipation performance

Under the liquid cooling conditions of the inlet coolant temperature of 298.15 K, flow rate of 0.4 L/min, and chip heat flow density of 100 W/cm², topology optimization—straight microchannel integrated cold plate (Case D)—can achieve the highest chip temperature compared with the traditional straight microchannel cold plate (Case A). High temperature reduction of 4.28 K, pressure drop reduction of 319.42 Pa, and improvement of temperature uniformity by reducing the temperature standard deviation TSD from 1.97 K to 1.20 K [9].

3. NoC architecture multi-dimensional optimization technology

3.1. Fault tolerance based on random forest - low power collaborative mapping model

3.1.1. Data set construction and model training

Use ANSYS Fluent to establish a conjugated heat transfer and flow numerical model of the heat dissipation system, use the hexahedral grid and carry out grid-independent verification; at an ambient temperature of 40 °C, the inlet is set to the speed entrance (such as 8 m/s), the outlet is set as the normal pressure outlet, and the equivalent heat source energy Under the conditions of release rate 2.0×107 W/m³, parametric comparative analysis is carried out by changing the TPMS structural height h1, wall thickness/porosity c1, thickness gradient t1 and wind speed v1, and based on the highest temperature of the heat source (Tmax), temperature distribution uniformity/temperature Poor indicators and system quality are used as the basis for comprehensive evaluation [4].

3.1.2. Performance test

In the heat dissipation verification of high-power chips, the proposed HP-GTPMS composite heat dissipation structure can achieve the maximum temperature reduction of the heat source, the improvement of temperature uniformity, and the reduction of the system weight of the system compared with the traditional aluminum straight-slot fin radiator; in the process of 300 s heat dissipation, the total heat dissipation of the system is also improved [4].

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3.2. NoC topology design adapted to quantum computing

3.2.1. HMRPD/HTRPD topological construction

This work is aimed at the wireless chip-to-chip concurrent transmission scenario in the package. It uses a TSV-like vertical unipolar antenna to establish a link, and introduces a channel-shortening filter with interference perception at the receiving end. By using multi-link joint statistical characteristics, it improves the detection end SINR and reduces BER, and there is no need for the cooperation of the transmitter [11].

3.2.2. Topological performance evaluation

This scheme is aimed at wireless chip-to-chip concurrent transmission in the package, adopts a TSV-like vertical unipolar antenna, and introduces a covariance regularized channel shortening filter (RI-CSF) for interference perception at the receiving end: before matching the filter, it is based on "all concurrent transmitters with The input covariance at the time of "activation" is learned, so as to jointly suppress ISI and multi-link interference under concurrent interference conditions, detect SINR after promotion and reduce BER (up to 10−5 magnitude at about 0 dBm) [11].

3.3. Channel shortening equalization technology of wireless NoC in the package

3.3.1. Interference perception channel shortening scheme

In response to the problems of retransmission and performance degradation caused by core failure in NoC, a fault-tolerant core mapping framework based on random forest is proposed, and Hamming code error detection/correction is used on the chip; when the failure persists, the faulty core task is migrated to the backup core to maintain operation and reduce retransmission and delay [5].

3.3.2. Performance verification

Numerical simulation and hardware implementation results show that the proposed fault-tolerant core mapping framework based on random forests is in a variety of Mesh NoC scales (such as 5×5 to 20×20) and workload evaluation. It introduces a Hamming code-based error detection and correction mechanism on the chip, and migrates the fault core task to the backup core when the failure continues, so as to reduce retransmission and improve system performance and energy efficiency. On the Zynq UltraScale+ MPSoC ZCU104 FPGA platform, compared with the adaptive mapping baseline, the area and power consumption are reduced by an average of 16% and 20.4% respectively, the throughput is increased by 24.2%, and the resource overhead (SLICE LUTS=30804) is lower [5].

4. CMOS-compatible on-chip energy storage device modification

4.1. Nitrogen-doped carbon nanotube pseusdocapacitor supercapacitor

4.1.1. Plasma doping process

Adopt a two-step plasma process: first introduce defects on the surface of carbon nanotubes through Ar plasma (200 W, -100 V bias), and then achieve nitrogen doping through N_2 plasma (200 W, 10 sccm flow rate) [3]. The performance evaluation results show that the proposed 2D/3D hybrid

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topology effectively improves the stability and bandwidth utilization of data transmission in the quantum interconnection environment. Compared with the traditional mesh network, the delay is reduced and the energy consumption is significantly optimized [6].

4.1.2. Electrochemical properties

The group delay of HTRPD in two-dimensional topology is lower than that of HMRPD; 3-D HTRPD in three-dimensional topology also has a lower delay and the highest throughput. In terms of energy consumption, 3-D HTRPD shows the largest energy overhead due to additional surround links, followed by 3-D HMRPD and 2-D HTRPD, and 2-D HMRPD has the lowest energy consumption [6].

4.2. ReRAM interface modification and performance improvement

4.2.1. Interface modification scheme

In response to the problem that the W electrode in the W/HfO_2 structure is prone to oxidation, which in turn affects the stability of the device, the literature stabilizes the interface WOx through 300℃ annealing of the O_2 atmosphere, and introduces a 3 nm Al_2O_3 diffusion blocking layer between W/HfO_2 to inhibit the cross-border migration of oxygen. TEM/EDX chemical analysis shows that the oxygen gradient at the interface after the introduction of Al_2O_3 is significantly weakened, indicating that it can effectively block the diffusion of oxygen to the W electrode side [7].

4.2.2. Resistance change property

After the introduction of 3 nm Al2O3, the resistance ratio of the device HRS/LRS can reach about 6, and the double-logmic I-V fitting shows that the conductivity conforms to the SCLC mechanism of trap control. The device shows the bipolar resistance of negative SET (about -1 V) and positive RESET (about 2–3 V); in 100 cycle tests, the resistance state tends to stabilize after about 40 times (HRS≈20 kΩ, LRS≈3 kΩ), and can be in 1 mA Realize a self-limiting flow operation of about -2 V/3 V under the condition [7].

5. Research on the heat dissipation performance of TIM, a gallium-based liquid metal

5.1. Thermal physical properties and theoretical models

Defect generation is decoupled from the nitrogen introduction process through two-step plasma treatment: first, Ar+ bombardment is used to form active sites such as empty/suspended bonds on the surface of CNT, and then the active nitrogen species are covalently bound at the defect site in the N2 plasma, to regulate the nitrogen bond configuration and improve the electrochemical activity and the contribution of the electrochemical activity of the electrode [3].

5.2. Experimental comparison and parameter optimization

Comparative tests in 1 mol·L-1 Na2SO4 electrolyte show that two-step plasma modification (Ar pretreatment introduction defect + N2 plasma nitrogen-adding) can significantly improve the performance of VACNT electrode capacitance; under optimized conditions, the sample surface capacitance can reach 34.2 m F·cm-2, the contribution of the false capacitance is about 47.87%.

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Raman shows that I_D/I_G is from 0.72 to 1.12 liters, and XPS shows that pyrrole nitrogen and quaternal nitrogen are the main doping configurations (about 68.94% and 15.62%) [3].

6. Conclusion

This paper reviews the research progress of high-power chip thermal management and on-chip interconnection/device collaboration optimization. In terms of multi-structure coupling heat dissipation, dry ice particle jet phase change cooling can obtain higher COP under system-level parameter optimization, and take into account safe temperature control and performance improvement under appropriate diffusion angle conditions; the TPMS-heat pipe composite heat dissipation structure shows lower peak temperatures at different wind speeds, and there is a more suitable wind speed. Working interval. In terms of interface materials, Ga-In liquid metal TIM can significantly reduce the temperature of the heat source under 90 W working conditions compared with traditional thermal silicone grease, and reveals the impact of key factors such as thickness and interface area on thermal properties. In terms of interconnection, congestion perception topologies such as HMRPD/HTRPD have advantages in terms of energy consumption and delay, and can be applied to quantum accelerator interconnection scenarios. In general, the existing work still lacks system-level collaborative design and long-term reliability data support for thermal management, interconnection and integrated devices. In the future, we can further explore the dynamic adaptive collaborative optimization framework and extreme environmental reliability assessment system for changes in working conditions.

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