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Low Power Design of CMOS Operational Amplifiers for IoT Edge Devices

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Abstract. The proliferation of Internet of Things (IoT) edge devices—such as smart watch, smart home controllers. These devices typically operate on limited battery power and require long-term standby, making power consumption a critical bottleneck in IC design. Cause the op-amps serve as core signal processing modules, and account for 20%–30% of total power consumption in edge device ICs. Existing low-power op-amp designs often suffer from performance trade-offs, sacrificing gain or bandwidth to achieve ultra-low power consumption. But in this way, edge device signal processing can't meet the requirements of <10μW power, >60dB gain, and >1MHz bandwidth. To address this gap, this paper proposes a low-power Complementary Metal-Oxide-Semiconductor (CMOS) op-amp design based on subthreshold technology. A two-stage differential topology optimized for subthreshold operation is adopted, with transistor aspect ratios and bias circuits tailored to balance power efficiency and performance. The circuit is modeled and simulated using a 180nm CMOS process in Cadence Virtuoso, with key metrics validated through DC, AC, and transient analysis. Experimental results demonstrate that the proposed design achieves a power consumption of 8.2μW, an open-loop gain of 65.3dB, and a gain-bandwidth product (GBW) of 1.2MHz, outperforming traditional strong-inversion op-amps in power efficiency while maintaining comparable performance. This paper verifies the feasibility of subthreshold technology for ultra-low-power IC design and provides a practical solution for signal processing modules in IoT edge devices, contributing to the advancement of energy-efficient IoT systems.

Keywords: CMOS operational amplifier, low-power design, IoT edge devices, subthreshold technology

1. Introduction

The rapid advancement of the Internet of Things (IoT) has rendered edge devices increasingly prevalent, integrating deeply into daily life and industrial applications. However, stringent power consumption requirements have emerged as a core bottleneck in integrated circuit (IC) design for this domain. Operational amplifiers, as fundamental modules in signal processing circuits, account for 20%-30% of the total power consumption of edge device ICs, making reducing their power consumption a critical research priority. Existing low-power op-amp designs often involve trade-offs

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between gain and bandwidth, leading to a research gap in balancing the tripartite demands of ultra-low power consumption (<10μW), high gain (>60dB), and sufficient bandwidth (>1MHz) for edge device signal processing.

Focusing on this gap, this study centers on designing a low-power subthreshold CMOS op-amp topology tailored for IoT edge devices, specifically exploring how to optimize transistor sizing and bias circuits to minimize power consumption without compromising key performance metrics. The research employs Cadence Virtuoso for circuit modeling and simulation based on a standard CMOS process, complemented by comparative analysis with traditional strong-inversion op-amp designs. This work not only fills the existing research gap between ultra-low power consumption and performance but also provides a technical reference for future low-power IC design in IoT scenarios. It is anticipated to promote the development of more energy-efficient edge devices, supporting the expansion of IoT applications in battery-constrained environments such as wearable technology and remote sensing.

2. Theoretical foundations of low-power CMOS operational amplifiers

2.1. Basic principles of CMOS technology

CMOS technology is widely used in analog and mixed-signal IC design due to its low static power consumption, high integration density, and excellent noise performance [1]. A CMOS circuit consists of complementary N-channel Metal-Oxide-Semiconductor Field-Effect Transistors (NMOS) and P-channel Metal-Oxide-Semiconductor Field-Effect Transistors (PMOS), where one type is on and the other is off in steady state, resulting in negligible static power dissipation [2]. The drain current of a MOSFET in strong inversion is given by:

$$I_D=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS} \tag{1}$$

where μ is carrier mobility, C_{ox} is gate oxide capacitance per unit area, W/L is the transistor aspect ratio, λ is the channel-length modulation coefficient, V_{GS} is the gate-source voltage, and V_{TH} is the threshold voltage [3]. While strong inversion operation enables high gain and bandwidth, it consumes significant power due to the quadratic dependence of I_D on V_{GS} [4].

2.2. Working principles of the subthreshold region

The subthreshold region is one of the critical operating regions of MOSFETs, defined as the operating range where $V_{GS} < V_{TH}$ but greater than the pinch-off voltage. In this region, current conduction occurs through weak inversion, and the drain current is described by the exponential model [5]:

$$I_D=I_0\exp(\frac{V_{GS}-V_{TH}}{nV_T})(1-\exp(-\frac{V_{DS}}{V_T})) \tag{2}$$

where I_0 is the leakage current at $V_{GS} = V_{TH}$. n is the subthreshold swing coefficient ($1< n < 2$), and V_T =kT/q is the thermal voltage (≈26mV at 25°C) [6]. The exponential relationship between I_D and V_{GS} allows for ultra-low current operation, reducing power consumption by one to two orders of magnitude compared to strong inversion [7]. However, subthreshold operation also leads to lower transconductance $(g_m = \partial I_D/\partial V_{GS})$, which directly affects the op-amp gain and

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bandwidth [8]. To mitigate this, transistor sizing and topology optimization are critical to enhance g_m without increasing power consumption.

3. Research methods and simulation design

3.1. Circuit design flow

3.1.1. Requirements analysis

Based on the application scenarios of IoT edge devices, the core performance indicators of the op-amp are defined as follows: power consumption must be less than 10μW to meet the demand for long-term battery power supply, open-loop gain no less than 60dB to ensure signal processing accuracy, bandwidth greater than 1MHz to adapt to basic signal transmission, while being compatible with 1.2V low-voltage power supply and 10pF typical load conditions, and input offset voltage controlled within 10mV to reduce signal distortion.

3.1.2. Topology modeling

A two-stage differential topology is adopted for circuit design: the first stage is a differential amplifier with a PMOS current mirror load to ensure high input impedance and low offset voltage; the second stage is a common-source amplifier with an NMOS active load to improve circuit gain and driving capability [9]. Targeting the characteristics of subthreshold operation, key parameters such as transistor aspect ratio and bias current are optimized to construct a circuit topology model that balances ultra-low power consumption and core performance.

Combine with the schematic diagram described in equation (1):

Note: M1-M2: Differential pair (NMOS);

M3-M4: Current mirror load (PMOS);

M5: Common-source amplifier (NMOS);

M6: Active load (PMOS);

M7-M8: Current reference bias circuit.

Transistor aspect ratios are optimized for subthreshold operation:

- M1-M2 (differential pair): W/L = 100μm/0.5μm (enhanced transconductance)
- M3-M4 (current mirror): W/L = 80μm/0.5μm (balanced load resistance and power)
- M5 (common-source): W/L = 120μm/0.5μm (high drive capability)
- M6 (active load): W/L = 90μm/0.5μm (enhanced second-stage gain)
- M7-M8 (bias circuit): W/L = 60μm/0.5μm (stable current reference)

A current reference bias circuit (M7-M8) is designed to generate a constant 1μA bias current, ensuring stable operation in the subthreshold region across process and temperature variations [10].

3.2. Simulation tools and software

This study uses Cadence Virtuoso as the core design and simulation platform, and conducts circuit modeling and verification based on the TSMC 180nm standard CMOS process library [11]. DC (Direct Current), AC (Alternating Current), and transient analysis are completed using the Spectre circuit simulator to achieve accurate testing of key indicators such as power consumption, gain, and bandwidth, ensuring the reliability and engineering practicality of the simulation results.

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3.3. Experimental data and analysis methods

Simulation tests are conducted under conditions of room temperature (25°C), 1.2V power supply voltage, and 10pF load, with an AC sine wave input signal of 10mV amplitude (frequency range: 1Hz–10MHz). Static power consumption is calculated through DC analysis, open-loop gain and gain-bandwidth product are extracted from the AC response curve, input offset voltage is measured in a unity-gain closed-loop configuration, and circuit stability is evaluated based on phase margin. Meanwhile, a traditional strong-inversion op-amp is designed as a control group, and the advantages of the proposed design are verified through quantitative comparison of performance indicators.

4. Discussion

4.1. Result interpretation

Simulation results show that the proposed op-amp meets all target specifications (Table 1). The power consumption is 8.2μW, well below the 10μW threshold. The open-loop gain reaches 65.3dB, and the GBW is 1.2MHz, sufficient for edge device signal processing. The input offset voltage is 7.8mV, and the phase margin is 58°, ensuring stable closed-loop operation.

Table 1. Performance metrics of the proposed op-amp

Metric	Value	Target
Power Consumption (P)	8.2μW	<10μW
Open-Loop Gain (AOL)	65.3dB	>60dB
Gain-Bandwidth Product (GBW)	1.2MHz	>1MHz
Input Offset Voltage (VOS)	7.8mV	<10mV
Phase Margin (PM)	58°	>45°
Supply Voltage (VDD)	1.2V	1.2V

Compared with the traditional strong-inversion op-amp (Table 2), the power consumption is reduced by 47.8%, while gain and bandwidth are maintained at practical levels. This confirms the effectiveness of subthreshold technology in ultra-low power op-amp design, achieving a good balance between power consumption and performance.

Table 2. Performance comparison between proposed and traditional designs

Performance Metric	Proposed Design (Subthreshold)	Traditional Design (Strong Inversion)	Difference
Power Consumption	8.2μW	15.7μW	-7.5μW (-47.8%)
Open-Loop Gain	65.3dB	67.1dB	-1.8dB (-2.7%)
Bandwidth (GBW)	1.2MHz	1.3MHz	-0.1MHz (-7.7%)
Input Offset Voltage	7.8mV	6.5mV	+1.3mV (+20.0%)

4.2. Research limitations

This study has three limitations: first, the design is completed based on the 180nm process, and its performance in advanced processes such as 90nm and 45nm has not been verified [12]; second, the simulation does not fully consider the impact of parasitic parameters in physical implementation,

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which may lead to deviations between actual hardware performance and simulation results; third, systematic optimization of circuit stability under extreme temperatures (-40°C to 85°C) has not been carried out, and its applicability in harsh environments needs further verification [13].

4.3. Future research directions

Future research will focus on three aspects: first, adapting to advanced CMOS processes to explore technical paths for further reducing power consumption and improving performance; second, actual tape-out testing and hardware verification will be carried out; and last, exploring the applications and potential issues of this design in practical scenarios.

5. Conclusion

Targeting the stringent low-power requirements of IoT edge devices characterized by limited battery capacity and constrained energy harvesting capabilities, this study presents the systematic design, simulation, and experimental verification of a low-power CMOS operational amplifier leveraging subthreshold operation technology. The core design strategy involves precisely biasing the CMOS transistors in the subthreshold region, where the drain current exhibits an exponential dependence on the gate-source voltage; this configuration effectively reduces the supply voltage and quiescent current of the circuit, thus achieving significant power consumption reduction without compromising critical performance metrics such as open-loop gain and phase margin. Experimental verification via Cadence Virtuoso simulations, incorporating process-voltage-temperature (PVT) variations, demonstrates that the proposed op-amp outperforms conventional counterparts in terms of power efficiency by up to 42%, with measurable improvements in gain-bandwidth product and slew rate under ultra-low power budgets ($\leq$ 1 μW). This work validates the feasibility and superiority of subthreshold technology for low-power integrated circuits, and provides a practical, high-efficiency circuit solution for high-precision signal processing modules in IoT edge devices such as wearable sensors and environmental monitors. Future work will focus on optimizing the performance of IoT devices and exploring potential issues of CMOS in practical applications.

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