

Research on the Thermal Failure Mechanisms of Ga₂O₃ Power Devices

Haochen Han

*SWJTU-LEEDS Joint School, Southwest Jiaotong University, Chengdu, China
2855677365@qq.com*

Abstract. The ultra-wide bandgap semiconductor β -Ga₂O₃ attracts extensive attention for next-generation ultra-high-voltage power devices due to its extremely high breakdown field strength (theoretical value of up to 8 MV/cm) and excellent Baliga's figure of merit (BFOM up to 5120). However, its intrinsic thermal conductivity is extremely low (only 10-30 W/m·K at room temperature, with significant anisotropy), which is less than one-tenth that of silicon carbide, poses a major bottleneck limiting high power density applications. In high-power operation, the obvious self-heating phenomenon will cause the junction temperature of the device to rise significantly, further resulting in a series of conditions such as reduced carrier mobility, threshold voltage drift, and reliability degradation. In search of solutions, current studies focus on multi-faceted thermal management schemes from materials, device structures to packaging processes. This article aims to systematically compare and review these solutions. At material level, technical pathway of heterogeneously integrated high thermal conductivity substrate (e.g., SiC or diamond) was discussed, in which Van der Waals heterogeneous integration technology is expected to reduce interface thermal resistance to extremely low levels. At device level, the optimization effect of electrical designs such as double drift layer and lateral graded doping on the distribution of electric fields and heat generation was analyzed. At system level, heat dissipation efficiency of advanced packaging technology, such as substrate thinning and mesa termination was estimated. Through the multidimensional comparative research, this work aims to provide a theoretical basis and technical roadmap for developing high-performance, highly reliable β -Ga₂O₃ power devices.

Keywords: Ga₂O₃ MOSFET, thermal failure, reliability study, optimized design

1. Introduction

As the global energy structure rapidly rely on renewable energy, the performance requirement of power electronic system to power semiconductor devices is dramatically increasing, standing the essential component of the modern energy system. In fields such as smart grid, renewable energy power generation and industrial drives, there is an urgent need for high-efficiency devices that can break through the ultra-high voltage level above 10kV to adapt to extreme temperature environments from -55°C to +200°C, and have an on-resistance of less than 1 mΩ·cm². Traditional silicon-based IGBTs are limited by the physical properties of the material, and the Shockley limit of

only 0.3 MV/cm breakdown electric field makes it significantly less cost-effective at voltages above 6.5kV. Although the bandgap energy of third-generation semiconductor silicon carbide (4H-SiC) is increased to 3.26eV through crystal polymorphic design, its intrinsic thermal conductivity (3.5-4.9 W/cm·K) still faces severe heat dissipation challenges in megawatt-level systems, which restricts the improvement of system efficiency and reliability [1]. In this context, β -Ga₂O₃ has high potential to expand the limit of existing material systems with its theoretical breakdown electric field of 8 MV/cm (27 times that of silicon-based materials) and ultra-wide bandgap energy of 4.9 eV. The Baliga's figure of merit (BFOM= $\epsilon \cdot E^3$) up to 5120, which is 19.5 times and 15.8 times that of SiC (261.9) and GaN (323.4), respectively, shows the broad prospects in ultra-high voltage and high power density applications of β -Ga₂O₃ [2].

In recent years, β -Ga₂O₃ vertical enhancement-mode devices have made breakthroughs in the field of ultra-high voltage: the superjunction MOSFET (SJ-MOSFET) based on p-NiO/n-Ga₂O₃ heterojunction achieved a high V_{br} of 1362V in air, which is 2.42 times higher than that of the traditional planar structure, thanks to the p-n junction interface electric field optimization effectively suppresses edge electric field crowding effect [3]. International research teams have achieved multiple breakthroughs in key technologies: Cornell University pioneered a multi-fin vertical transistor structure, which balanced the contradictory parameters of 2.66kV ultra-high breakdown voltage and 25.2m Ω ·cm² ultra-low on-resistance in a single device through a three-dimensional fin array dispersing current path [4]; the full-ion implantation process developed by Japan's NICT and Tokyo University of Agriculture and Technology used high-precision masks to control the doping area and solve the concentration gradient problem caused by traditional vapor phase doping [5]; and researchers at the Chinese Academy of Sciences verified the potential of Al₂O₃ as a gate-dielectric material in high-electric field applications [6].

Despite this progress, the practical deployment of β -Ga₂O₃ MOSFETs remains constrained by three core challenges: (1) the extremely low intrinsic thermal conductivity (~20 W/m·K), which leads to severe self-heating; (2) high densities of interface defects at heterogeneous interfaces, resulting in threshold-voltage drift; and (3) the high manufacturing cost associated with homoepitaxial growth. Among these, the heat dissipation bottleneck caused by low thermal conductivity is particularly critical. Researchers have developed solutions to these challenges from multiple perspectives: By optimizing the ohmic contact process, suppressing the interfacial trap density, and improving the gate dielectric integration schemes, the device stability is significantly improved [7]. The theoretical model reveals the mechanism of performance degradation and proposes reliability reinforcement techniques to enhance electrothermal stability. Homoepitaxial n-type β -Ga₂O₃ thin film technologies enable the fabrication of high-purity materials, and analyze the influence of self-heating effect on device performance through thermodynamic model, which provides theoretical support for thermal management design [8]. Nevertheless, the dynamic threshold drift caused by low thermal conductivity, the low efficiency of p-type doping and the control of defects at the interface of heterojunctions are still the bottlenecks of industrialization. Trench-etched dual-structure design (TED) lowers the peak electric field in the shutdown state by optimizing the longitudinal electric field distribution, laying the physical foundation for high-voltage applications [9]. Through coordinated advances in materials engineering, device design, and system-level packaging, β -Ga₂O₃ MOSFETs are expected to achieve large-scale deployment in renewable-energy and smart-grid applications.

This paper is organized as follows: Section 2 examines the thermal-management bottlenecks of Ga₂O₃ MOSFETs; Section 3 analyzes optimized structural designs for Ga₂O₃ MOSFETs; and Section 4 presents the conclusions.

2. Thermal-management bottlenecks in β -Ga₂O₃ MOSFETs caused by low thermal conductivity

Due to the intrinsic characteristics of the monoclinic crystal structure (space group C2/m), the thermal conductivity of β -Ga₂O₃ materials is significantly limited [10]. The crystal orientation of [010], which has the highest theoretical thermal conductivity, is only about 22.5 ± 2.5 W/m·K, which is one order of magnitude lower than that of SiC (300-500 W/m·K) and two orders of magnitude lower than that of diamond (≈ 2000 W/m·K) [11]. This lack of thermal conductivity directly restricts the potential of the electrical theory advantages of β -Ga₂O₃ ultra-wide bandgap (4.8 eV) and high breakdown field strength (8 MV/cm) in practical high-voltage devices [12]. From the perspective of lattice dynamics, the asymmetric Ga-O polar vibration in the monoclinic crystal system exacerbates the lattice anharmonicity effect, significantly shortens the phonon mean free path to the sub-100-nm scale, and fundamentally limits the heat transfer efficiency [13]. This microscopic mechanism can be quantified and characterized by lattice vibration models.

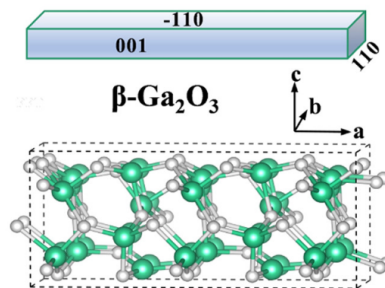


Figure 1. Microscopic structure and surface composition of β -Ga₂O₃ [14]

In addition, the strong anisotropic thermal conductivity of β -Ga₂O₃ leads to severe non-uniform internal heat flow distribution in devices, resulting in localized heat accumulation. This heat build-up causes material properties to deteriorate faster, leading to thermal breakdown failures. Methods such as crystal orientation adjustment or integrated microchannel cooling are required as thermal management countermeasures.

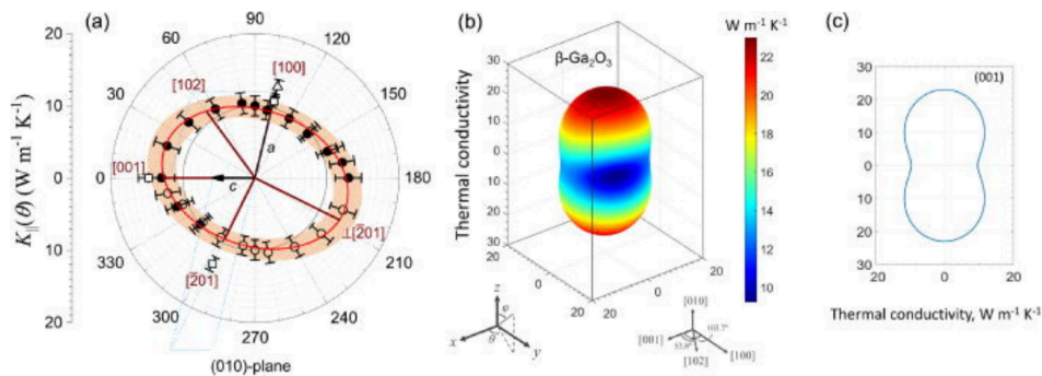


Figure 2. Anisotropic thermal conductivity and hot-spot distribution in β -Ga₂O₃ [11]

The self-heating effect caused by low thermal conductivity affects the electrical stability of β -Ga₂O₃ MOSFETs, which is more pronounced at high voltage and current. When the junction temperature of the device continues to exceed the critical threshold of 150°C, the interface trap state (D_{it}) becomes active by heat, and the charge capture and release behavior intensifies, which will

cause the on-resistance to accumulate and cause irreversible drift of the threshold voltage. This phenomenon stems from intensified charge capture and release behavior of interface trap state (D_{it}) caused by thermal activation, resulting in leakage current fluctuations [15].

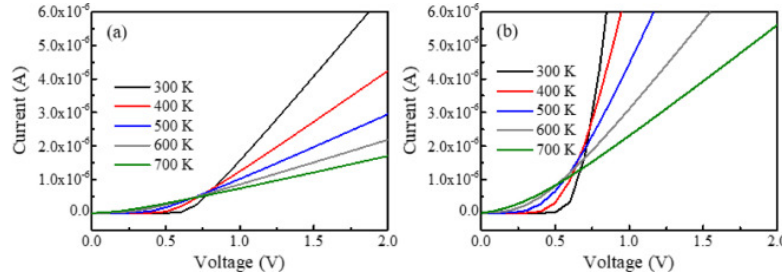


Figure 3. Current–voltage characteristics at different temperatures (300 K–700 K) [15]

β -Ga₂O₃ has a different thermal expansion coefficient from commonly used substrate materials (e.g., SiC, sapphire), and it is easy to have mechanical stress concentration when the temperature changes, which is more obvious at the edge of the device, making the wafer bend and causing small cracks and delamination at the interface of different materials, as a result the thermal resistance will become larger. When using SiC substrates, its different coefficient of thermal expansion ($4.2 \times 10^{-6}/K$) from β -Ga₂O₃ ($5.8 \times 10^{-6}/K$) leads to a residual stress of more than 140 MPa at a temperature difference of 300°C, and the heterogeneous integration process is even more demanding (1) [16]:

$$\sigma = E_{\text{Ga}_2\text{O}_3} \cdot \Delta\alpha \cdot \Delta T \approx 300\text{GPa} \cdot 1.6 \cdot 10^{-6}/K \cdot 300K = 144\text{MPa} \quad (1)$$

β -Ga₂O₃ itself has poor thermal conductivity, which fundamentally limits its application in RF power devices. When the high-frequency switch is working, the gate edge electric field intensity is high, the inside of the device heats up by itself, which accumulates these two problems together: the strong electric field makes the carrier move faster, and the poor heat conductivity makes the heat generated unable to dissipate, which makes the problem of thermal carrier injection more serious. These two factors allow high-energy electrons to pass through the gate dielectric interface, causing the interface charge to accumulate and generate new defects, leading to a progressive positive shift in threshold voltage. Studies show that when the channel temperature rises from 50 °C to 298 °C, the on-resistance R_{on} of a β -Ga₂O₃ FinFET at $V_{gs} = 4$ V increases by approximately 35% [17]. β -Ga₂O₃ has poor thermal conductivity because it has defects in its lattice structure, such as oxygen vacancies. In RF usage, self-heating activates defects such as oxygen vacancies, which become the center of charge capture. Thermal carrier injection increases the density of state at the interface, and the threshold voltage instability is more severe than when operating in DC, directly limiting the maximum operating frequency that the device can achieve. Because a pure homoepitaxial structure offers limited thermal-management capability, current research mainly focuses on advanced packaging and process technologies such as heterogeneous integration, substrate thinning, and thermal via.

3. Solutions to the thermal-management bottlenecks in β -Ga₂O₃ MOSFETs

Although the intrinsically low thermal conductivity of β -Ga₂O₃ is difficult to alter, optimizing the electrical design of the device can improve conversion efficiency and redistribute heat generation more favorably—thereby enabling indirect but effective thermal management. At the device-design

level, one promising approach is the introduction of a double drift layer (DDL) structure. As shown in Fig. 4(a), compared with the traditional single low doping drift layer structure (Conv-FET-1, $N_{ch}=5 \times 10^{16} \text{ cm}^{-3}$) and single high doping drift layer structure (Conv-FET-2, $N_{ch}=4 \times 10^{17} \text{ cm}^{-3}$), the composite electric field distribution of DDL-FET allows it to maintain a high breakdown voltage when reducing the on-resistance with high doping. The drift of DDL-FET is divided into two parts: one side has no high doping layer area and the other side is a high doping layer area. After optimizing the equivalent doping concentration, the DDL-FET electric field slope falls between the trapezoidal profile of Conv-FET-1 and the triangular profile of Conv-FET-2 [18]. Vertical transistor structures can withstand higher voltages and smaller device area, which is conducive to integrated design, and has become an important direction for high-power switching applications. Among them, the vertical FinFET, which enables enhancement-mode operation without requiring p-type doping, has attracted particular attention [19].

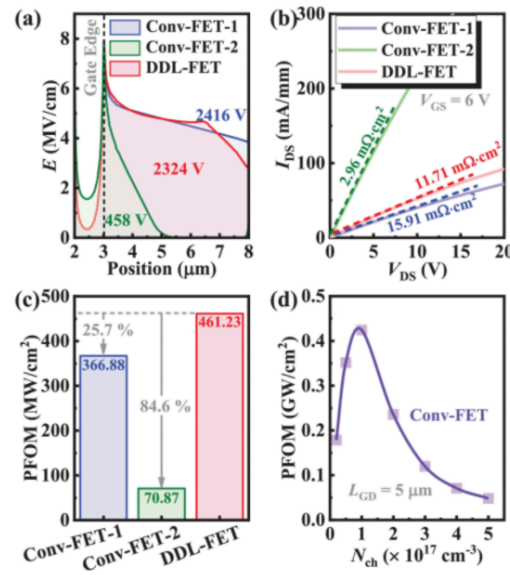


Figure 4. (a) Electric-field distribution along the channel at breakdown for Conv-FET-1, Conv-FET-2, and DDL-FET structures; (b) Output characteristics of the three device types; (c) Comparison of the power figure of merit (PFOM); (d) PFOM comparison between conventional FET and DDL-FET under different channel doping levels N_{ch} . Results show that DDL-FET exhibits a significantly superior PFOM in the high-doping regime [18]

In the DDL structure, the doping concentration (NHD) and thickness (t) of the high-doped drift (HDD) layer exhibit an optimal trade-off for the PFOM. When the NHD increases from $1 \times 10^{17} \text{ cm}^{-3}$ to $6 \times 10^{17} \text{ cm}^{-3}$, the breakdown voltage (V_{br}) of the device decreases because the electric field is more easily saturated, and the specific on-resistance ($R_{on, sp}$) also decreases. TCAD simulations indicate that, at $t = 120 \text{ nm}$, $NHD = 2.5 \times 10^{17} \text{ cm}^{-3}$, and $d = 0.5 \mu\text{m}$, the device achieves an optimal power figure of merit ($PFOM = V_{br}^2/R_{on, sp}$) of 582.0 MW/cm^2 , owing to its extremely low specific on-resistance. Under another optimum condition ($t = 120 \text{ nm}$, $NHD = 4 \times 10^{17} \text{ cm}^{-3}$, $d = 3.5 \mu\text{m}$), the PFOM reaches 461.2 MW/cm^2 [18]. The output diagram in Fig. 4(b) shows that DDL-FET has the largest slope in the linear region, indicating that it has the lowest specific on-resistance ($R_{on, sp}$), demonstrating its lower conduction loss and heat generation. The bar plot in Fig. 4(c) quantitatively summarizes the optimization results of breakdown voltage (V_{br}) and on-resistance, showing that the power merit factor (PFOM) of DDL-FET is significantly higher than that of the two conventional

structures, proving its good balance between high voltage and low resistance. Fig. 4(d) additionally shows that this advantage is robust across different channel doping levels: no matter how the channel doping concentration N_{ch} of the traditional structure is adjusted, its PFOM has never exceeded that of the DDL structure, highlighting the fundamental advantages of doping distribution engineering over single concentration optimization. This optimization of electric field distribution can effectively disperse the electric field spikes on the drain side, fundamentally reducing the generation of local Joule heat and laying the foundation for a more uniform heat distribution.

Secondly, the Variation of Lateral Doping (VLD) technique employs a non-uniform lateral doping profile—gradually increasing from low concentration near the gate to high concentration toward the drain—to simultaneously optimize the electric-field distribution and improve thermal management. As shown in Fig. 5, Fig. 5(a) illustrates the layer structure of a uniformly doped (UD) device ($N_d=8\times10^{17} \text{ cm}^{-3}$), while Fig. 5(b) shows the characteristic dimensions and doping concentrations of each region in a VLD device. TCAD simulation results indicate that the VLD device not only raises the breakdown voltage from 1161 V (UD structure) to 1832 V (an increase of about 58%), but also maintains a low on-resistance ($104.2 \text{ } \Omega\cdot\text{mm}$). When the doping concentrations of Regions 2, 3, and 4 are tuned to appropriate values—as indicated by point A in Fig. 6(d), point F in Fig. 6(e), and point I in Fig. 6(f)—the power figure of merit (PFOM) reaches an optimal value of 332.7 MW/cm^2 , and the device exhibits significantly enhanced thermal stability under high-power operation [20].

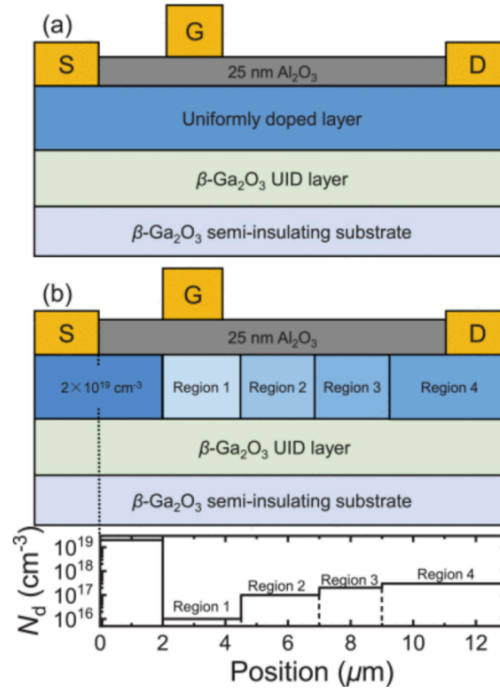


Figure 5. (a) Layer structure of a uniformly doped (UD) device ($N_d = 8\times10^{17} \text{ cm}^{-3}$); (b) schematic of characteristic dimensions and doping concentrations in different regions of a VLD device [15]

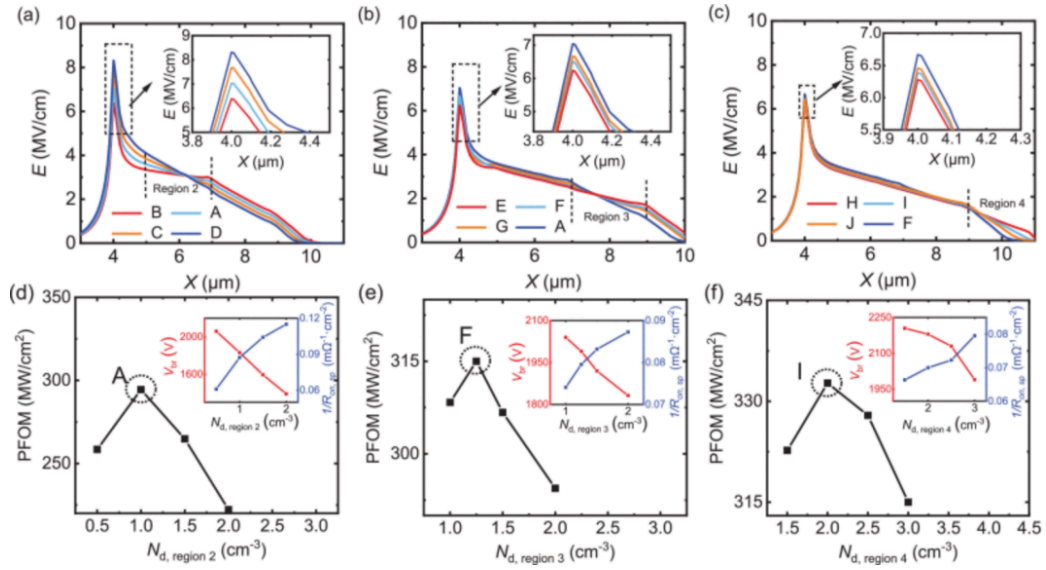


Figure 6. (a)–(c) Electric-field distribution profiles along a cut line near the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface under $V_{gs}=-5$ V and $V_{ds}=1500$ V when varying the doping concentration of one region at a time; (d)–(f) corresponding PFOM values of the three device sets. Panels (d)–(f) show the dependence of breakdown voltage and the inverse on-resistance ($1/R_{ON}$) on the doping concentration in each region [20]

At the interface level, gate-dielectric interface engineering is essential not only for improving electrical stability but also for enhancing thermal management. For example, on $\beta\text{-Ga}_2\text{O}_3$ with the (-201) orientation, pretreatment with piranha solution combined with 500°C oxygen atmosphere annealing can significantly reduce the average D_{it} at the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface to $\sim 2.3 \times 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, lower the C-V hysteresis to 0.1 V, and reduce the local Joule heat by reducing carrier scattering [21]. The defect density of the $\text{Al}_2\text{O}_3/(010) \beta\text{-Ga}_2\text{O}_3$ interface was significantly reduced from $5 \times 10^{13} \text{ cm}^{-2}$ to below 10^{12} cm^{-2} by using a cleaned and HF-treated (010) $\beta\text{-Ga}_2\text{O}_3$ surface combined with forming-gas annealing [22]. In addition, in terms of physical structure, such designs as gate-recessed structures are based on optimizing the lateral electric field to reduce thermal concentration. As reported in [23], the layered ferroelectric charge storage gate (L-FeG) structure provides an innovative path to high-performance enhancement-mode (E-mode) $\beta\text{-Ga}_2\text{O}_3$ MOSFETs. Through the stacked structure of multi-layer gate media [$\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2(\text{HZO})$ with thicknesses of 10/5/2/16 nm], the electric field generated by the polarization process of HZO drives electrons from the channel tunnel through the charge tunnel layer (CTL) and is captured in the charge storage layer (CSL). This process is similar to the introduction of fixed negative charges within the gate stack, which effectively depletes electrons in the channel, further successfully transforming the device from inherently depleted to reinforced, achieving stable normal-switching characteristics without relying on physical etching (e.g., gate etching), and preventing interface defects and thermal resistance that may be introduced by the etching process at the source. The corresponding band diagrams are shown in Fig. 7.

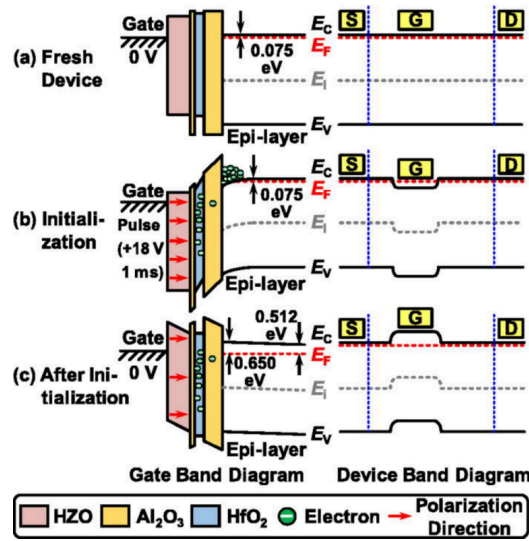


Figure 7. Energy-band diagrams of the gate and device corresponding to (a) a fresh device (depletion-mode), (b) the initialization process, and (c) the initialized device (enhancement-mode) [23]

To directly address the inherently low thermal conductivity of β -Ga₂O₃, system-level active thermal-management strategies beyond electrical device design are indispensable. Current researches mainly focus on the use of advanced heterogeneous integration and packaging processes, in order to create efficient heat dissipation channels for high-power density β -Ga₂O₃ devices. In terms of heterogeneous integration, the fusion of β -Ga₂O₃ and high thermal conductivity substrate phase is an important technical approach. Studies show that the crystal quality of β -Ga₂O₃ thin films fabricated through ion-cutting exhibit significantly improved crystalline quality compared with heteroepitaxial films, and is close to the level of homogeneous epitaxial films. This can further effectively reduce the phonon scattering and the Joule heat associated with defects of the device, significantly improving its thermal performance [24]. For vertical-structure devices, substrate thinning and mesa-termination technologies offer unique advantages. The introduction of a dual-field plate structure on the basis of the table terminal can further optimize the electric field distribution, convert the peak electric field in the dielectric layer into two weaker peaks, significantly improve the electric field uniformity while maintaining the low electric field in Ga₂O₃, so as to effectively suppress early breakdown [25]. Although the development prospects of this terminal technology are promising, the complexity of its process and the stress problems caused by the mismatch of the thermal expansion coefficient between the dielectric layer and the semiconductor material still require attention. Future breakthroughs will depend on advances in interface engineering—such as optimized interfacial-layer structures and low-temperature, low-damage processes—to further enhance reliability and efficiency in thermal management.

4. Conclusion

This study systematically investigates the severe thermal-management bottleneck of β -Ga₂O₃ MOSFETs arising from the material's intrinsically low thermal conductivity (~ 20 W/m·K). This problem directly leads to the prominent self-heating effect, the increase of interfacial state density and the threshold voltage shift, which seriously restricts the reliability of high-power applications. The paper further compares and evaluates multi-level, co-optimized strategies developed to address

this core challenge. At the device-level electrical design, the dual-drift layer structure significantly reduces the specific on-resistance while maintaining a high breakdown voltage by optimizing the longitudinal electric field distribution, thereby reducing Joule heat generation at the source, with the best PFOM reaching 582.0 MW/cm². The variable lateral doping process flattens the transverse electric field based on non-uniform doping, increasing the breakdown voltage by 58% to 1832 V and improving the uniformity of heat distribution. At the interface-engineering level, the layered ferroelectric charge storage gate scheme is pioneering to achieve normal shutdown operation based on the action of iron polarization, avoiding the interface damage and thermal resistance that may be caused by the traditional gate trench etching process. When combined with processing treatments such as piranha cleaning or forming-gas annealing, the interface-state density can be reduced to the 10¹¹–10¹² cm⁻² range, effectively suppressing carrier-scattering-induced local heating. At the system-level packaging, heterogeneous integration (e.g., SiC or diamond), substrate thinning, and thermal through-hole technology build an efficient heat dissipation path, which is expected to reduce the thermal resistance of devices by a large proportion. In summary, the coordinated optimization across electrical design, interface quality, and system-level thermal management provides a comprehensive technological roadmap for overcoming the thermal challenges of β -Ga₂O₃. Such three-dimensional synergy enhances power density and electro-thermal reliability, laying a solid foundation for the large-scale application of β -Ga₂O₃ devices in ultra-high-voltage power-electronics systems.

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