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High-Density Static Random Access Memory Circuits Design

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Abstract. Advanced Internet of Things (IOT), electronic devices are trending toward miniaturization. Contemporary System-on-Chip (SoC) implementations demand both high density and superior energy efficiency. As a critical building block in SoC systems, Static Random Access Memory (SRAM) is widely adopted due to its outstanding symmetric characteristics, superior stability and low power consumption. High-density SRAM is critical to optimizing SOC performance and area efficiency, making its design an essential research focus. This paper focuses on the circuit design of high-density SRAM, conducting an in-depth exploration of key design technologies, including SRAM optimization based on advanced CMOS processes like FinFET, the development of high-accuracy sense amplifiers and the research of peripheral circuit assist technologies for improving read/write yield and energy efficiency. It also summarizes the current development status of high-density SRAM circuits and puts forward feasible research directions for its future advancement, providing technical references for high-density SRAM design adapted to IOT and advanced SOC applications.

Keywords: High-density SRAM, CMOS technology, Sense amplifier, Peripheral circuit, SOC

1. Introduction

In recent years, IOT technology has witnessed an explosive development, placing increasingly high demands on area efficiency and performance of SOC design. In SOC design, memory occupies a large portion of the area in an SOC. Hence, Memory design directly affects the overall chip area and performance. SOC chips utilize various types of memory, which can be classified according to functionality into Read Only Memory (ROM) and Random Access Memory (RAM). ROM's data was stored after a power loss, whereas RAM does not. Due to its random-access capability, RAM is widely adopted. Based on different storage principles, Traditional RAM includes SRAM and Dynamic Random Access Memory (DRAM). DRAM concentrates on simpler internal storage cells with fewer transistors and a smaller footprint compares to SRAM, which are primarily used in computers as high-capacity storage devices. Although SRAM's basic memory cells consist of multiple transistors and thus cannot achieve the same high density as DRAM. Its high write and read speed, CMOS process compatibility and high energy efficiency let SRAM plays an ideal role for low-power IOT applications, which satisfies high-performance and easy to integrate into mainstream chip manufacturing's characteristics.

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As the transistor feature size continues to shrink, SRAM is experiencing severe leakage problems. Compared with DRAM and other emerging memories like STT-MRAM and ReRAM, the conventional 6T SRAM bitcell itself has relatively low area efficiency. In the face of such problems, modern industry often uses advanced CMOS compensation. Similarly, high-density SRAM storage arrays have large parasitic resistor capacitance and large capacity, which affects the success rate of SRAM read and write operations. To solve this problem, the mainstream methods are bitcell design, advanced sensitive amplifier design and peripheral auxiliary circuit design. This paper will discuss several existing designs for high-density SRAM which include SRAM design based on advanced CMOS technology, sensitive amplifiers with high accuracy and peripheral auxiliary circuit research. Furthermore, this paper summarizes the current development of high-density SRAM circuits and provides feasible ideas for future research.

2. Preliminary

SRAM constitutes a form of volatile semiconductor memory using bistable flip-flop circuits to store data. SRAM does not need to be periodically refreshed to preserve data, enabling SRAM to achieve high read/write speed, low access latency and strong noise immunity. Figure 1 shows the basic 6T SRAM structure [1].

The 6-transistor (6T) SRAM structure is the most widely used storage cell structure in modern SRAM designs. Data storage is realized by a bistable flip-flop that consists of dual cross-coupled CMOS inverters labeled M1 to M4. A pair of NMOS access transistors (M5-M6) are gated through wordline to link internal storage nodes to the external bitlines. The cross-coupled inverters maintain two complementary and stable states, corresponding to logic 1 and logic 0. The wordline (WL) is used to select or deselect cell, while the bitline (BL) and complementary Bitline (BLB) are responsible for data input during write operations and data sensing during read operations.

The read operation flow can be described as the following processes. BL and BLB precharge to VDD to the same high level before reading. The address decoder activates WL, turning on access transistors M5 and M6 to connect Q/QB to BL/BLB. One bitline discharges slowly, forming a small voltage difference. The sense amplifier amplifies this discrepancy to a full logic level and outputs valid data. After data latching, WL is disabled, and bitlines are precharged again. The stored data remains unchanged during reading.

The write operation can be described as the following processes. The write driver sets BL and BLB to complementary voltages based on input data. Write 1 set BL equals to VDD, BLB equals to VSS. Write 0 set BL equals to VSS, BLB equals to VDD. WL is enabled to turn on M5 and M6, connecting bitlines to Q/QB. Strong bit-line voltages overcome cross-coupled inverter feedback, forcing Q/QB to flip and overwrite data. After stabilization, WL is disabled, inverters hold the new data, bitlines precharge, and the cell enters hold mode [1].

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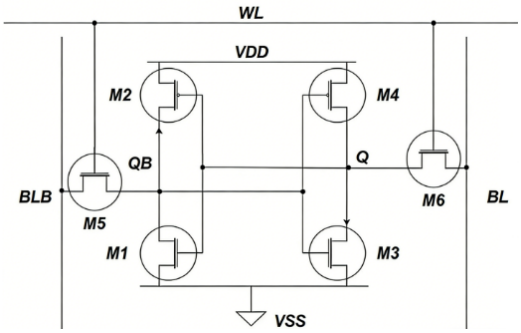

Figure 1. 6T SRAM [1]

3. High-density compatible SRAM design

3.1. SRAM design and research system based on advanced CMOS technology

With the continuous advancement of CMOS technology, the feature size of CMOS devices has been steadily shrinking, which strongly drives the development of SRAM toward high-density design. However, as the CMOS feature size scales down, the leakage current issue in SRAM has become increasingly severe. Emerging CMOS technologies offer effective solutions to this challenge, with FinFET being the typical representative.

Intel Corporation proposed the high-density bitcell using Intel 4 CMOS technology, the High Density Cell (HDC) cell is designed to density up to 0.0240 μm^2 , adopting PU:PG:PD with 1:1:1 fin ratio to enhance driving capability [2]. In 2021 IEDM, Samsung Electronics shows the 4nm FinFET platform (4LPE), obtains 7-10% performance improvement and 12% power reduction compared with the 5nm platform by using Transistor Level Design Technology Co-Optimization (T-DTCO) technology, the Ultra-High-Density (UHD) SRAM cell maintains equivalent Static Noise Margin (SNM) and V_{MIN} distribution while achieving area scaling, it enables direct current (DC) components and alternative current (AC) components, achieving 50% of total boosting [3]. In 2023, Taiwan Semiconductor Manufacturing Company (TSMC) designs 0.021 μm^2 HDC and High-Current Cell (HCC) to reduce 30% area of peripheral logic and improve 10% for N3 SRAM macro area [4].

3.2. Design of high-accuracy SARM sense amplifier

As the core module of SRAM read operations, the read margin of sense amplifier directly determines the sense of amplifier's detection accuracy and anti-interference ability. International Business Machines Corporation (IBM) proposed a Single-ended SAs (SESA), it dynamically adjusts bias voltages (V_{B_N} , V_{BL} , V_{B_P}) via a programmable DC bias generator to adapt to different Process, Voltage and Temperature (PVT) conditions, the shmoo plot shows that it can operate at 2GHz under 0.5V supply and 6.2GHz under 1.0V supply, demonstrating excellent wide-voltage and high-frequency performance [5]. TSMC proposed the Sense-Amplifier Enable signal Interlock (SAEI) circuit in 2024 ISSCC, which disconnects the data lines (DL, DLB) from the precharged data lines (PDL, PDLB) immediately after the sense amplifier is activated, shortening the read duration and enabling rapid bitline precharge [6]. The Offset Voltage (V_{OS}) has a great influence on sensing delay and energy consumption in SRAM. In 2023, Kwangwoon university proposed to store the offset voltage in a capacitor by using Single-ended Offset Canceling Sense Amplifier (SOSA), which achieves 5.83% mean standard deviation and 15% average sensing delay, finally reducing 2.2

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times σ_{OS} compared with the existing technology [7]. Body Biased Hybrid Sense Amplifier (BHSA) was proposed in TCAS-II in 2025, it uses feedback loop, connects the bitline to the NMOS on opposing sides of the sense amplifier, achieving the lowest σ_{OS} compared with traditional sense amplifier like Hybrid Latch Sense Amplifier (HYSA) and Bit-Blind Sense Amplifier (BBSA) [8].

3.3. Research on peripheral circuit assist technologies of SRAM

Peripheral auxiliary circuit plays an important role in SRAM. A good peripheral circuit design can effectively improve the reading and writing accuracy of SRAM. In 2021 ISSCC, Samsung Electronics proposed the SRAM assist circuits, Adaptive Dual Bit Line (ADBL) and Adaptive Cell-Power (ACP), which improve the write margin by using R_{VDDC} for bitcell position differences, advancing the SRAM ability [9]. Yonsei University and Articron proposed Self-Enabled Write-Assist Cell (SEWAC) in 2024 ISSCC which adopts a cell-compatible layout design, embedding the write-assist circuit into the memory cell array, meeting the 6 σ write yield at $R_{BL_cell} = 120\Omega$ without additional timing control signals to deal with the exponential growth of interconnect resistance in advanced FinFET processes, SEWAC constructs an additional write path between memory cells without relying on timing control signals and dummy cells, it achieves 100% write yield at $R_{BL_cell} = 240\Omega$, showing better write capability improvement than traditional Flying BL (FBL) and Dual Bit Line (DBL) schemes [10]. Intel corporation proposes an architecture that eliminates half-selected cell's wasted power through Column-Mux 1 (CM1) design when the high bandwidth 6T SRAM array design (6T-HBW) was applied, enabling the read assist circuit disabled through write operations which expands the V_{MIN} operating window and achieves better low-voltage adaptability, reducing bitline capacitance by 40% [2]. TSMC proposed the pseudo-2-port SRAM, it adopts a double-pumping architecture, combining WL-negating shortcut-control (WNSC) clock generator and real-time dynamic performance scaling (RTDPS) technology, achieving 4.3GHz operating frequency at 1.0V and 100℃, with a Figure of Merit (FOM) of 90.7GHz/ mm^2 /V [6]. TSMC proposed the Selective Negative Bit Line (SNBL) technology in Very Large Scale Integration (VLSI) in 2023, the SNBL technology triggers negative Bit Line (NBL) bias detects write failure, avoiding full-cycle power loss of traditional NBL write-assist which ensures a 6 σ requirement even in ultra-low voltage less than 0.6V scenarios [4]. Tsinghua University proposed the Voltage Boosted Fail Detecting-Selective Cell Current Boosting (VBFD-SCCB) circuit, it selectively boosts the cell current (ICELL) by detecting the bitline discharge state of slow cells, shortening the detection time of the sense amplifier by 36% and significantly improving read accuracy at low voltages [11]. In 2025 ISSCC, TSMC shows the sense amplifier coordinates with the NBL write-assist scheme, placing the Far-End Precharge (FE-PRE) module at the bitline far end to enhance the precharge strength of long bitlines and cooperate with the Far-End Write-Assist (FE-WA) module to double the bitline precharge speed, avoiding voltage deviation in far-end cell read detection, solving the NBL voltage loss problem in the long bitline of the 1024 pseudo-row architecture and cooperating with the FE-PRE module to realize the high-density array design of 512 cells [12].

4. Conclusion

This paper mainly focuses on analyzing the current challenges and the feasible solutions in existing high-density SRAM designs. With the rapid development of integrated circuits and SoC applications, the performance requirements for SRAM have become increasingly stringent. The integration of advanced CMOS processes, high-accuracy sensing circuits and efficient peripheral auxiliary technologies has effectively broken through the traditional technical bottlenecks of SRAM,

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promoting its continuous development toward ultra-scaled feature sizes. This integrated optimization scheme can well meet the strict requirements of area efficiency and overall performance in modern SoC design. These research results will provide important technical supports for the development of highintegration SOC systems, and further help highdensity SRAM play an increasingly important role in the field of IOT.

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