

The Role of CMOS Technology in Modern Microprocessor Design: A Review

Zeyu Yao

*Department of Electric and Electrical Engineering, University of Birmingham, Birmingham, UK
yzy0510202023@163.com*

Abstract. The rapid advancement of computing systems demands the development of low-power, high-speed microprocessors. Due to its scalability, low power dissipation, and high efficiency, CMOS has emerged as one of the important technologies in semiconductor engineering. This review explores the importance of CMOS technology in the design of modern microprocessors. CMOS VLSI design offers the circuit design of modern logic circuits and memories used to create advanced processor architecture. While CMOS scaling improves the transistor density and performance of microprocessors it also introduces significant design complexity. CMOS technology has also enabled the design of multi-core and chiplet processors. However, modern CMOS-based processors suffer from several challenges such as energy consumption, increased leakage currents, heating, limited scalability, and design complexity. This study concludes that while CMOS technology plays an important role in the creation of modern processors, future advancements require the use of innovative techniques in design at device, circuit, and architecture levels.

Keywords: CMOS Technology, Microprocessor Design, VLSI Design, Power Efficiency, Chiplet-Based Processors

1. Introduction

As a key computing component in electronic systems, microprocessors are widely used in devices including personal computers, mobile devices, industrial control systems, and Internet of Things (IoT) applications. Processor performance improvements have long been closely tied to advances in semiconductor technology, particularly complementary metal-oxide-semiconductor (CMOS) technology. Benefiting from its advantages in energy efficiency, integration density and process scalability, CMOS underpins the modern integrated circuit (IC) industry [1]. Moreover, continuous CMOS scaling has paved the way for the trend described by Moore's Law: the number of transistors integrated on a single chip grows steadily over time [1].

Current research has emphasized the critical role of CMOS technology in modern microprocessor design. Studies on advanced CMOS devices show that three-dimensional transistor structures, such as Fin Field-Effect Transistor (FinFET) and Gate-All-Around Field Effect Transistor (GAAFET), can effectively improve device performance [1]. Other work traces the evolution of processors from early commercial models such as the Intel 4004 and Intel 8086, and links architectural progress to semiconductor technology advances [2, 3]. Research on CMOS power consumption, Very Large-

Scale Integration (VLSI) design and chiplet-based processors indicates that modern microprocessor development relies on more factors beyond transistor scaling alone [4-6].

However, existing studies lack a systematic review of CMOS technology and microprocessor architecture spanning from process and circuit levels to system-level integration. To address this gap, this paper analyzes the contributions of CMOS technology to contemporary microprocessor design from three core dimensions: the co-evolution of CMOS and VLSI technologies, the impact of CMOS on processor performance and power efficiency, and the support of CMOS for advanced architectures such as multi-core and chiplet designs. This work aims to provide insights into how CMOS technology can continue to enable future microprocessor development.

2. Theoretical foundations

2.1. Basic CMOS device structure and VLSI fundamentals

CMOS technology is built on complementary pairs of n-type (NMOS) and p-type (PMOS) transistors. In steady-state logic operation, only one transistor in the pair conducts at a time, creating no direct current path between the power supply and ground. This complementary switching mechanism is the fundamental basis of low-power digital circuits [7].

Powered by CMOS technology, Very Large Scale Integration (VLSI) enables the integration of massive numbers of logic gates and memory cells on a single chip. Continuous CMOS process scaling steadily improves VLSI integration density, laying the circuit-level foundation for increasingly complex processor architectures.

2.2. CMOS power consumption basics

Power consumption is a core constraint in CMOS processor design. Modern processors integrate billions of transistors in a tiny area, so the power dissipation of a single transistor is significantly amplified at the chip level. CMOS power consumption is divided into two main categories: dynamic power dissipation and static power dissipation [4].

2.2.1. Dynamic power consumption

Dynamic power dissipation accounts for the majority of power consumption in modern high-speed processors. It arises from logic state transitions in CMOS circuits during operation. When signal levels switch between 0 and 1, output nodes and internal parasitic capacitances are repeatedly charged and discharged. Dynamic power is determined by switching activity, parasitic capacitance, supply voltage and operating frequency. Since dynamic power scales with the square of supply voltage, voltage reduction is an effective way to lower power consumption [4].

2.2.2. Static power consumption

Static power dissipation is mainly caused by subthreshold leakage current when transistors remain in a steady off state. Ideally, static power should be negligible, as one transistor in the NMOS/PMOS pair is turned off under stable logic states [5]. In practice, leakage power exists even when transistors are inactive [4]. With advancing transistor scaling, static power has become a growing concern. Shrinking device dimensions weaken the ability to suppress current flow, aggravating leakage issues. The main contributors to leakage current are subthreshold leakage, gate leakage and junction leakage [4].

3. Impact of CMOS technology on modern microprocessor design

3.1. Development of microprocessor architecture

Continuous CMOS device scaling has played a vital role in achieving higher transistor density and more complex processor architectures. It enables the integration of more transistors on a single chip, which in turn supports larger cache capacities, wider datapaths, control circuits and multi-core processing units [1, 2]. This scaling trend aligns directly with Moore's Law, making CMOS miniaturization far more than a manufacturing-level improvement [1].

The evolution of microprocessors is closely tied to advances in semiconductor devices and integrated circuits. Early commercial processors represented by the Intel 4004 laid the technical foundation for modern processor design, despite limited transistor count, low operating frequency and simplified instruction sets [2, 3]. Driven by technology advances, mainstream processors have evolved from 4-bit and 8-bit architectures to 16-bit, 32-bit and eventually 64-bit high-performance designs. The Intel 8086, for example, adopted an independent Bus Interface Unit and Execution Unit to improve operating efficiency [2].

To further optimize instruction execution efficiency, the Reduced Instruction Set Computer (RISC) architecture has been widely adopted for simplified instruction scheduling and optimized pipeline design [2]. Meanwhile, auxiliary modules including caches, memory management units and floating-point units have been integrated into processor chips thanks to high-density CMOS VLSI. Instead of relying solely on clock frequency improvement, modern processor design has shifted toward parallel computing, realizing the transition from single-core to multi-core and advanced multi-die systems.

3.2. Impact on processor performance

At the circuit level, processor performance is directly determined by transistor switching speed. As CMOS transistors scale down and switch faster, circuit delay is reduced. Processor clock frequency is constrained by the longest critical path of internal circuitry, so improvements in CMOS switching speed directly enable higher clock frequency and faster processing. In this sense, CMOS technology boosts processor performance both by increasing transistor integration density and by accelerating internal circuit operation.

Furthermore, faster CMOS circuits support deeper pipeline designs. By dividing instruction processing into stages including fetch, decode, execution, memory access and write-back, reduced per-stage latency allows deeper pipeline implementation, which enables parallel processing of multiple instructions across stages and improves overall instruction throughput [2].

3.3. Impact on power efficiency

Power efficiency is a critical constraint in contemporary microprocessor design. As performance improvement relies on more complex circuits, wider datapaths, deeper pipelines and additional functional units, excessive static power would cause severe overheating and exceed power budgets. Despite increasing transistor counts per chip, CMOS circuits maintain relatively high energy efficiency. This feature allows processor designers to pursue higher performance through architectural optimization without power consumption going out of control.

3.4. Impact on system-level integration and architecture complexity

CMOS technology has been instrumental in improving system integration and the architectural complexity of modern microprocessors. The increased number of transistors resulting from CMOS scaling provides a basis for constructing more complex processor architectures. Beyond basic arithmetic and control units, more complex architectures can now be integrated into processors, which include on-board cache memories, large data paths, memory-based units, and more sophisticated execution units [5]. Close on-chip integration also reduces data transfer latency between different parts of the device, improving overall system efficiency.

An evolution of cache memory can serve as an illustration for this trend in integration. As processor speeds increased, memory access became the limiting factor, and integrating cache memory on or near the chip itself alleviated this by providing the processing unit with storage for frequently accessed data. These examples demonstrate that CMOS technology enabled the incorporation of memory-based structures into chip system design.

In recent years, processor integration has shifted from a monolithic single-die processor to chiplet-based architectures. Rather than using a single large die, chiplet processors consist of many smaller dies packaged together [6]. The advantage of this type of processor is that more cores can be included while simultaneously improving manufacturing yield across different sections of the processor. Examples of modern chiplets and tile processors include AMD EPYC Milan, Intel Sapphire Rapids, and ARM Graviton 3 [6]. In summary, CMOS technology drives integration progress at both the circuit and system levels. The process of scaling down CMOS technology enables greater transistor density and functionality, but other technologies, such as advanced packaging and chiplets, have helped push beyond single-chip limits. This trend has helped make modern processors more powerful.

4. Discussion

4.1. Limitations of CMOS-based processor design

Despite CMOS technology's significant contributions to microprocessor development, its future advancement faces multiple inherent challenges.

The marginal benefits of continuous CMOS scaling are diminishing with each generation. While earlier technology nodes delivered simultaneous improvements in transistor density, switching speed and cost, scaling has now approached physical limits at the nanometer scale, making further miniaturization increasingly difficult and expensive [1]. Short-channel effects, leakage currents and thermal issues largely offset the performance gains from pure geometry shrinking. Aggressive scaling introduces growing device reliability risks. The aggressive thinning of gate dielectrics in advanced nodes leads to uniform tunnelling-current-induced photon emission in ultra-thin gate oxides even under normal operating conditions. Localised defects can concentrate current at weak spots and trigger dielectric breakdown, shortening device lifetime and raising stricter requirements for fault isolation in technology qualification [8]. Hot carrier injection (HCI) also induces a gradual threshold voltage shift and transconductance degradation, becoming a major constraint on processor lifespan at advanced nodes.

Meanwhile, parasitic latch-up, an inherent risk of the CMOS PNP structure, poses a more severe threat to high-density chips, as it can trigger destructive, sustained high-current states once activated. Power dissipation has become a critical bottleneck. Modern CMOS processors integrate billions of transistors, requiring careful management of both dynamic and static power during circuit

design [4]. Higher transistor density improves computing capability, but also increases thermal density and makes heat dissipation more challenging. As a result, performance cannot be improved solely by increasing clock frequency or transistor count. Growing system integration introduces new complexity. As chips incorporate more cores, caching, memory controllers, and special-purpose units, achieving efficient transistor use becomes harder. Communication latency, cache coherence, memory bandwidth and thermal management all become prominent constraints. Modern processor development cannot rely solely on transistor scaling; system-level integration optimization must also be addressed.

4.2. Future directions

Future CMOS microprocessor development should follow multiple complementary technical paths. New transistor designs, such as FinFET and GAAFET transistors, will continue to evolve. These designs ensure better electrostatic control and reduce leakage currents, unlike planar transistors [1]. In future generations, GAAFET designs may enable better gate control and allow CMOS devices to remain scalable for longer. However, these new designs also introduce higher fabrication complexity and rising design costs.

While FinFET and GAAFET represent the continued evolution of silicon-based CMOS, the ultimate limits of silicon may necessitate a transition to novel channel materials. Two-dimensional (2D) semiconductors have emerged as promising candidates for ultimately scaled transistors. For example, single-layer phosphorene, a 2D p-type semiconductor, exhibits a direct bandgap and high hole mobility at room temperature. When combined with n-type 2D materials, functional 2D CMOS inverters have been successfully fabricated, verifying that the complementary logic paradigm can be sustained on atomic-thin channels. Such material-level innovations could extend the CMOS technology roadmap beyond the silicon era [7].

Chiplet-based processor architectures will increasingly be used to address the limitations of large monolithic dies. This technique can help increase manufacturing yield and enable more cores per processor. In addition, future processor design will require greater collaboration among device technology, circuit design, and architecture. As the benefits of pure CMOS scaling diminish, performance is increasingly driven by the combination of advanced CMOS devices and architectural innovation

5. Conclusion

The purpose of the review is to analyze the contribution of CMOS technology to contemporary microprocessors. It becomes clear that CMOS technology offers the basic building blocks necessary for digital logic circuitry and allows for large scale integration required in contemporary microprocessors. Due to CMOS scaling and the application of VLSI technology, modern microprocessors have transformed from primitive one-chip microprocessors to more sophisticated microprocessors. Power efficiency made possible by CMOS technology is vital for contemporary systems as well.

But there are shortcomings to this review as well. The current study relies heavily on literature reviews only; no experiments have been conducted, no simulations carried out, and no quantitative analysis comparing the different processor technologies has been included in the paper. Moreover, this paper concentrates only on the advancement of CMOS processors. Further work can examine other transistor structures, like the FinFET or GAAFET, comparing their performance and effects on leakages. Additionally, more emphasis should be given to studies involving chiplet-based processors

and heterogenous integration. All in all, the future of CMOS technology looks very promising for use in microprocessor applications; however, it will be dependent on the joint evolution of devices, circuits, and architectures.

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