

Research on Architecture and Key Technologies of Low-Voltage and Low-Power CMOS Voltage References

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Abstract. With the explosive growth of the Internet of Things, wearable devices, implantable medical electronics, and wireless sensor networks, battery-powered systems impose increasingly stringent requirements on battery life and supply voltage. CMOS voltage references, as core building blocks of analog and mixed-signal ICs, have low-voltage and low-power characteristics that directly dictate the endurance and performance limits of IoT terminals and wearables. Based on subthreshold MOS device characteristics, this paper systematically reviews the core theories, mainstream architectures, and key optimization techniques of low-voltage low-power CMOS voltage references, compares the performance boundaries and application constraints of different circuit schemes, and summarizes the core technical bottlenecks in current designs. Research demonstrates that all-MOS subthreshold architectures can realize nanowatt power consumption and sub-1V operation, while DIBL effect compensation, high-order temperature compensation, and high PSRR design constitute the core technical paths to improving reference stability. These conclusions can offer theoretical reference and practical basis for the design of low-voltage low-power voltage references.

Keywords: CMOS voltage reference, low-voltage low-power, subthreshold circuit, temperature coefficient, power supply rejection ratio

1. Introduction

Portable wearables, wireless sensor nodes, and IoT terminals impose increasingly strict low-voltage, low-power demands on power management. CMOS voltage references, as core analog building blocks, determine system performance limits through output accuracy, power, and PSRR [1]. Conventional bandgap references based on BJTs cannot easily break the 1 V barrier; resistors and op-amps introduce significant power and area overhead, failing to meet sub-1 V and nanowatt requirements [2, 3].

Against this background, all-CMOS subthreshold references have attracted attention for lower voltage, nanowatt power, and improved stability/PSRR. This paper systematically reviews core theories, mainstream architectures, key optimizations, and typical achievements, summarizes current bottlenecks, and provides a comprehensive reference and insights for developing novel low-voltage low-power references.

2. Core theoretical foundations of CMOS voltage references

2.1. Key performance evaluation metrics

Voltage references are evaluated by power, stability, and robustness. Key metrics: temperature coefficient [1, 4]:

$$TC = \frac{V_{Ref,max} - V_{Ref,min}}{V_{Ref,average} \times (T_{max} - T_{min})} \times 10^6 \quad (1)$$

$$PSRR = 20 \lg \left(\frac{\Delta V_{DD}}{\Delta V_{Ref}} \right) \quad (2)$$

Quiescent power (pW–nW), minimum supply (sub-0.5V feasible), and process robustness via Monte Carlo [1, 5].

2.2. Core operating principles of low-voltage and low-power references

Low-voltage low-power designs rely on subthreshold MOS operation. When the drain-source voltage of a MOS transistor satisfies $V_{DS} > 4V_T$ (where $V_T = \frac{k_B T}{q}$ is the thermal voltage, approximately 26 mV at room temperature), the device operates in the subthreshold saturation region. The drain current formula is expressed as Equation (3) [1, 2, 4]:

$$I_{DS} = \mu C_{ox} \frac{W}{L} (\eta - 1) V_T^2 e^{\left(\frac{V_{GS} - V_{TH}}{\eta V_T} \right)} \quad (3)$$

In the formula, μ stands for carrier mobility, C_{ox} is the gate oxide capacitance per unit area, $\frac{W}{L}$ denotes the aspect ratio of the transistor, η is the subthreshold slope factor, and V_{TH} refers to the threshold voltage of the device.

The gate-source voltage of a subthreshold MOS consists of negative-TC V_{TH} and positive-TC V_T . Device sizing cancels these coefficients, producing a near-zero temperature-coefficient output [1, 6].

Current-mirror accuracy follows

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \beta}{\beta} + \frac{g_m}{I_D} \Delta V_T \quad (4)$$

where both current-factor and threshold mismatches must be addressed in advanced nodes [5].

3. Low-voltage low-power CMOS voltage references: mainstream architectures and research progress

According to topology and implementation, low-voltage low-power CMOS references are classified as all-MOS subthreshold, self-biased op-amp-free, and multi-output integrated. Their characteristics and developments are outlined in the following.

3.1. All-MOS subthreshold voltage references

As the mainstream architecture for low-voltage low-power applications, all-MOS subthreshold references eliminate the BJTs and large-value resistors of conventional bandgaps, relying solely on

subthreshold MOS transistors for temperature compensation, which significantly reduces power, shrinks area, and supports sub-1 V supply [1, 3].

Some researchers, using a novel self-biased current mirror in a 65 nm process, achieved a power consumption of 801 nW, a low temperature coefficient of 11.3 ppm/°C (−60 °C to 110 °C), and a low-frequency PSRR of 38 dB [1].

Another study proposed a resistor-less and BJT-free self-biased subthreshold reference that achieves temperature compensation by exploiting the threshold voltage difference between thick-oxide and thin-oxide NMOS transistors, realizing an ultra-low power consumption of 1.32 nW in a 65 nm process and mitigating performance fluctuations caused by process variations through 4-bit trimming [3]. Figure 1 shows the schematic of the proposed voltage reference and the self-biased NMOSFET voltage reference.

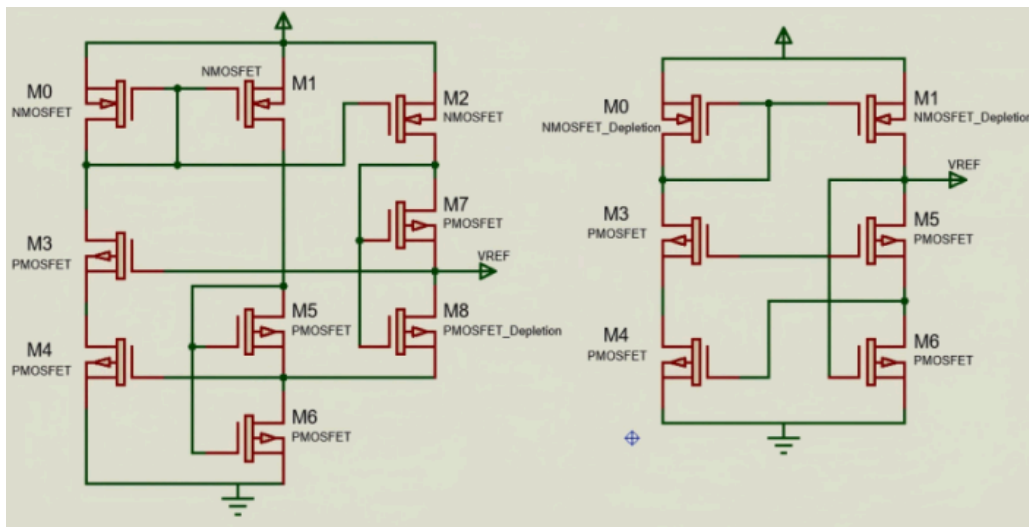


Figure 1. Schematic of the (a) proposed voltage reference, and (b) self-biased NMOSFET voltage reference

3.2. Self-biased op-amp-free low-voltage references

While op-amps enhance PSRR in conventional references, they introduce power overhead, stability design complexity, and low-voltage limitations. Op-amp-free architectures using self-biasing and closed-loop feedback simplify the circuit, reduce power, and still achieve good stability [7, 8].

Some researchers have proposed an op-amp-free reference with DIBL effect compensation, which achieves a minimum supply voltage of 0.34 V, a quiescent power of 48 pW, and a line regulation as low as 0.019%/V in a 0.18 μm process, representing a landmark achievement in picowatt-level references [7].

Other studies have adopted native devices to realize an op-amp-free dual-output reference with a power consumption of only 1.18 nW, suitable for low-power systems requiring multiple reference levels [8].

3.3. Multi-output and high-drive-capability reference architectures

To meet energy-harvesting and multi-module supply needs, multi-output and load-drivable references are critical, enabling single-chip multiple outputs and reducing system overhead [2, 6, 9]. One team exploited zero-/standard-threshold V_{th} difference and pre-regulation to achieve 1.3-nW

power in 0.18- μm CMOS, with -70-dB PSRR at 1 MHz [6]. Another proposed a 1-mA-load-drive CMOS reference via gate-voltage compensation (no buffer), featuring 10-nA quiescent current, 33.09-ppm/ $^{\circ}\text{C}$ TC over -20 – 140 $^{\circ}\text{C}$, and stable output from 1 μA to 1 mA, overcoming weak-drive limitations [9].

3.4. Key optimization techniques

To further enhance the temperature stability, supply noise rejection, and process robustness of voltage references under the constraints of low voltage and low power, researchers have proposed a variety of targeted optimization techniques. The core technical paths are as follows:

3.5. Temperature coefficient compensation optimization techniques

Temperature coefficient (TC) is a key performance metric. Compensation techniques fall into three types. First-order compensation cancels linear TCs of V_{TH} and V_{T} via aspect-ratio design; it is simple and low-power but struggles to achieve $\text{TC} < 20$ ppm/ $^{\circ}\text{C}$ [1, 3]. High-order curvature compensation suppresses nonlinear drift using piecewise or curvature correction—e.g., a modified Ogney current source generating T^2 -proportional bias achieved 19.3 ppm/ $^{\circ}\text{C}$ at 3.64 nW in 65 nm [10]. Trimming and calibration compensate process-induced TC drift via on-chip trimming.

3.6. Power supply noise rejection techniques

At low voltages, supply noise affects output. PSRR optimization relies on pre-regulation (isolating fluctuations), feedback loops (e.g., a gate-voltage loop achieving -63 dB at 5 Hz and load drive [9]), and high-impedance current mirrors with cascode/long-channel to suppress modulation and DIBL—a cascode mirror improves a 2-T reference's 100-Hz PSRR from -53 to -81.5 dB and line regulation [4]. Figure 2 shows the 2-T CVR evolution; the cascode mirror is key.

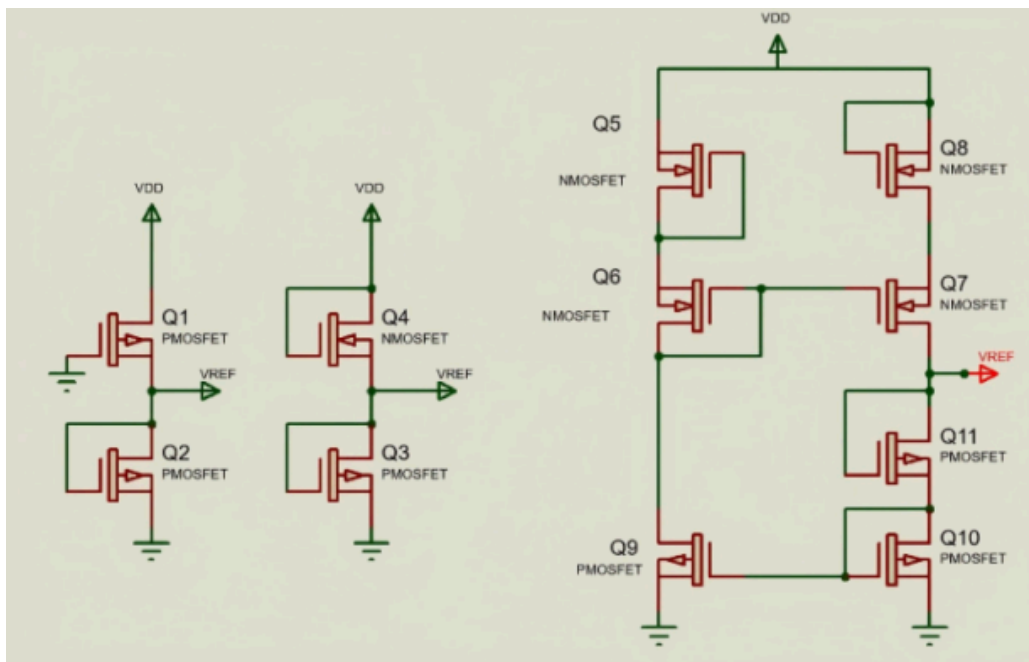


Figure 2. Schematic of (a) conventional 2-T CVR used in [9], (b) 2-T CVR using MVT pMOS and (c) proposed CVR based on 2-T

3.7. Process variation suppression techniques

In advanced CMOS processes, random mismatches in device threshold voltage and aspect ratio lead to dispersion of the reference output. Process variation suppression techniques mainly include:

Device matching design: Reducing transistor random mismatch through common-centroid layout, cross-coupling, and increasing device area. Studies have shown that increasing device channel length can simultaneously reduce both threshold voltage mismatch and current factor mismatch, thereby improving the current copying accuracy of current mirrors. This serves as a fundamental means to enhance the process robustness of voltage references [5].

Taking a 5V NMOS current mirror as an example, Figure 3 presents its Monte Carlo simulation results under 200 runs. The mirrored current exhibits a normal distribution with a mean of 1.000 μA and a standard deviation of 34.969 nA. Although these results are obtained from a 5V device, the underlying mismatch principles—such as the combined effect of threshold voltage and current factor mismatch—are equally applicable to low-voltage CMOS designs.

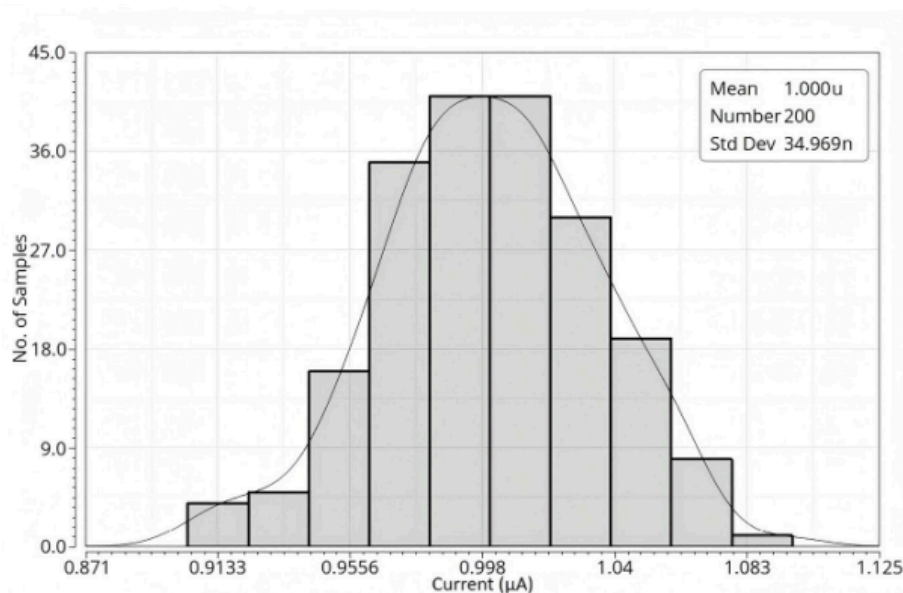


Figure 3. Statistical distribution of current deviation for the 5V nMOS mirror

On-chip trimming techniques: On-chip trimming techniques correct output offset and temperature drift caused by process variations through digital or analog trimming, which can significantly improve process consistency [1-3]. **Closed-loop self-calibration techniques:** Through self-biased and negative feedback structures, the sensitivity of the output to device parameter deviations is reduced.

3.8. Low-power and low-voltage adaptation techniques

For nanowatt, sub-1 V IoT requirements, key optimization techniques include:

All-device subthreshold biasing: Biasing all MOSFETs in subthreshold achieves nA-level currents, reducing quiescent power [1, 3, 7]. This has enabled pW–nW quiescent power and a 0.34 V minimum supply [7].

Resistor-less and op-amp-free architectures: Removing large resistors and op-amps cuts power and area overhead while eliminating op-amp low-voltage limits. Such designs achieve lower voltage and power with simplified circuitry [7, 11].

DIBL effect compensation: Complementary structures cancel DIBL-induced current drift in short-channel low-voltage devices. By exploiting the positive temperature coefficient of the DIBL effect in a complementary branch, supply-dependent bias current variation is cancelled, maintaining excellent line regulation even at ultra-low supply [7].

4. Technical bottlenecks and challenges of low-voltage low-power CMOS voltage references

Despite excellent low-power performance, key bottlenecks remain: power-accuracy-area trade-offs (mitigated via simplified architectures, compensation, and trimming); sub-0.5 V robustness issues (addressed by DIBL compensation, self-biased loops, and dedicated start-up); advanced-node short-channel and leakage effects (handled by matching and exploiting oxide-thickness V_{th} differences); and extreme-environment degradation (countered by curvature compensation, trimming, and pre-regulation).

5. Conclusion

This paper reviews low-voltage low-power CMOS voltage references, covering theories, architectures, optimizations, and bottlenecks. All-CMOS subthreshold designs eliminate BJTs/resistors via device temperature matching, achieving nW-pW power and sub-1 V operation. Architectures include power-efficient all-MOS, self-biased op-amp-free and multi-output/high-drive topologies. Key optimizations—high-order compensation, pre-regulation, DIBL suppression, and trimming—improve TC, line regulation and PSRR. Remaining challenges are the power-accuracy trade-off [1, 3], low-voltage robustness, advanced-node device limitations, and extreme-environment degradation. This work consolidates achievements, traces evolution, and offers design insights.

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