Proceedings of CONF-CDS 2026 Symposium: Computer Vision-Based Multimodal Cognitive Load Estimation for Adaptive Media Communication
DOI: 10.54254/2755-2721/2026.GL36151

The Deceleration of Moore's Law and Shifting Driving Forces of Microprocessor Technology: A Bibliometric Quantitative Analysis Based on Top IEEE Conferences

Congxi Shen

Maynooth International Engineering College, Fuzhou University, Fuzhou, China
CONGXI.SHEN.2026@mumail.ie

Abstract. As the size of transistors approaches the physical limit, Moore's Law, after nearly six decades, faces a fundamental limit. What will drive microprocessor technology in the post-Moore era is a key question for both industry and academia. Based on the top conference paper data from IEEE Xplore Digital Library from 2015 to 2025, this paper uses the bibliometric method to divide technological innovation driving forces into three dimensions: process-driven (Class A), architecture-driven (Class B), and advanced packaging and new paradigm-driven (Class C). Through precise search and annual statistics of publication volumes, and quantitative comparisons, the study found that the number of Class A papers remained highly stable over 11 years, indicating that the research on process miniaturization has entered a plateau stage; the number of Class B papers increased from 381 to 3437, and the ratio of B/A attention value soared from 5.4 in 2015 to 35.8 in 2025, indicating that architectural innovation has irreversibly replaced process miniaturization and has become the absolute main engine in the post-Moore era; the absolute quantity of Class C papers continued to grow, but its relative share decreased from 1.4 to 0.6, presenting a pattern of "steady supplementation rather than replacement of the mainstream". These quantitative results show the shift of technological drivers and provide empirical evidence for strategic planning and resource allocation.

Keywords: Post-Moore era, Architecture innovation, Bibliometric analysis, Microprocessor, Drive force migration

1. Introduction

Since Gordon Moore made his famous prediction in 1965, the semiconductor industry has experienced rapid growth over the past 60 years. By reducing the size of transistors, processors have achieved better performance and energy efficiency periodically, while also reducing their costs. This pattern was later referred to as "Moore's Law" [1]. However, as transistors shrink, physical bottlenecks (e.g., quantum tunneling and heat dissipation) have become more evident, and simply reducing size can no longer drive the industry as fast as before [2, 3]. It is widely recognized that the "More Moore" approach, where performance gains came purely from process upgrades, is winding down [3].

DOI: 10.54254/2755-2721/2026.GL36151

Nevertheless, the slowdown of the traditional Moore's Law has not hindered the development of microprocessors. Notably, over the past eleven years, computing performance has continued to increase. Process technology has advanced slowly, yet processor performance has not slowed accordingly. Therefore, the central question for academia and industry is what drives microprocessor progress in this era. Several qualitative analyses have proposed some viewpoints. Hennessy and Patterson pointed out that the computer architecture has entered a "new golden age", domain-specific architectures (DSA), chip-level design, and software-hardware co-design have become new driving forces [4]. While Shaff emphasized that new architectures, advanced packaging, and synergy among CMOS devices are strengthening and will replace simple process technologies [5].

These viewpoints are quite influential, but most of them still remain at the qualitative level, mostly based on expert opinions rather than objective data. Currently, few systematic quantitative evaluations have been conducted that track how the core driving forces have changed through analyzing published results. This study aims to fill this gap. This study conducted a bibliometric analysis of IEEE conference papers from 2015 to 2025. This study classified the driving factors into three categories and obtained annual paper counts and proportions, which produced a data graph of the shifting driving forces. This result truly reflects the transformation of driving forces and can provide data references for relevant enterprises and research institutions in resource allocation or technology route planning.

2. Data and bibliometric methodology

2.1. Data source and retrieval rules

IEEE Xplore is the sole data source, and the observation window is 2015-2025, covering the post-Moore era to the present. At the methodological level, this study follows the bibliometric analysis framework for scientific output growth proposed by Bornmann and Mutz, as well as the theoretical discussion on academic publication statistics by Garfield [6, 7]. The annual publication volume is regarded as the key indicator for measuring the level of attention to processor development in this study.

Three search query groups were run in this title field. Each group has different search keywords and limits the search scope to the paper titles. This restriction is beneficial for matching articles related to technology-driven topics, thereby reducing irrelevant results, but it may cause the omission of papers with broader titles. However, it drastically cuts down the time cost of literature collection and enables us to sort out the general trends of the research field.

Category A: process-driven. This group covers process scaling and front-end technology. Its terms include "FinFET," "GAA," "Gate-All-Around," "Nanosheet," "CMOS scaling," "technology node." This study combined these with qualifiers like "logic," "high performance," "SoC," "microprocessor" to narrow things down. Power devices, sensors, and photonics papers were excluded.

Category B: architecture-driven. This type of literature focuses on microarchitecture and system-level design.Terms include "architecture," "accelerator," "chiplet," "in-memory computing,""domain-specific,""dataflow," paired with computing-related qualifiers like "processor," "SoC," "compute," "deep learning." The same non-computing exclusions were applied.

Category C: advanced packaging and new paradigms. Its terms cover "silicon photonics," "quantum computing,""memristor," "neuromorphic," "heterogeneous integration," "advanced packaging," "2D material," again combined with computing-oriented qualifiers.

DOI: 10.54254/2755-2721/2026.GL36151

All three searches excluded sensors, power semiconductors, biomedical devices, flexible electronics, and other off-topic records. Each query was run separately for every year from 2015 to 2025, and matching conference articles were counted.

2.2. Three-category classification framework

The three groups follow the process, architecture, and Beyond-Moore paths described in the IRDS roadmap [8] and related discussions of post-Moore computing [5]. They are analytical lenses rather than an exhaustive or mutually exclusive taxonomy. This classification method has been widely adopted and is often used as a framework for analyzing the development of microprocessors after Moore's Law..

Category A: Process-driven. This category includes papers concerned with process control and front-end manufacturing, and it remains aligned with the classic "Moore's Law" development path [1]. Research in this group attempts to extend the physical limits of lithography, device structure, and process integration. Since its performance gains arise mainly from advances in materials and manufacturing, continued feature-size reduction remains a central objective.

Category B: Architecture-oriented. Papers in this category address innovation at the architectural level. Since Hennessy and Patterson identified DSA and software-hardware co-design as new performance drivers [4], researchers have increasingly examined the organization of computing, data transmission, and control processes. Rather than depending only on higher integration density, this approach seeks to use architectural design to make each transistor operate more efficiently.

Category C: Advanced packaging and new paradigms-driven. This category covers heterogeneous integration, advanced packaging, non-traditional CMOS devices, and emerging computing paradigms. Within the IRDS framework, these studies are generally classified as "Beyond Moore" research [8]. Their scope is broader than that of the other two categories and includes several promising exploratory paths. Nevertheless, such work has not yet become dominant in the field.

Taken together, these three categories form a consistent, literature-based framework for examining how the focus of research has changed over the past decade. Because the same classification criteria can be applied throughout the period, annual comparisons can be made without repeatedly recalibrating the rules.

3. Quantitative statistical results & core findings

3.1. Annual publication trend of three technical tracks

Table 1 lists the quantities of categories A, B and C from 2015 to 2025. Figure 1 presents the same data in a line graph to better illustrate the development trend.

Table 1. The number of papers published in various categories over a period of 11 years

	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
A	71	64	70	72	59	75	64	61	63	68	96
B	381	467	522	646	918	1062	1417	1541	1886	2481	3437
C	622	688	744	913	924	951	1008	1279	1498	1786	2167

DOI: 10.54254/2755-2721/2026.GL36151

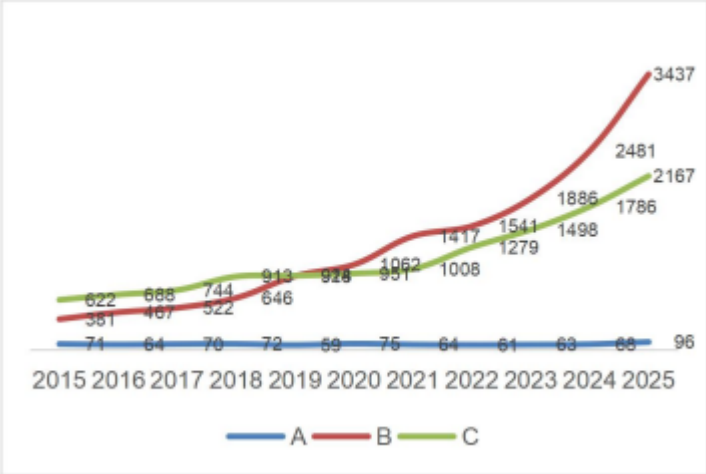

Figure 1. Line chart of yearly paper counts by category

Overall, the development paths of these three categories are significantly different. The papers of category A maintained a relatively stable level over the 11 years, fluctuating narrowly between 59 and 96. There was no obvious upward or downward trend. This indicates that research output based on transistor control has reached a plateau, and academic investment in this field has stabilized.

In contrast, Category B papers expanded rapidly. Their number rose from 381 in 2015 to 3,437 in 2025, making the 2025 total 9.02 times the 2015 level. This growth was uneven rather than continuous: it became noticeably faster after 2019, followed by a particularly sharp 38.5% increase from 2024 to 2025. The timing broadly coincides with the rapid scaling of large AI models—from GPT-2 (1.5B parameters) in 2019 to GPT-3 (175B) in 2020 and Llama-3.1 (405B) in 2024—which has driven an unprecedented demand for computational capacity and, in turn, spurred architectural innovation. Class C (advanced packaging and new paradigms) also grew from 622 papers in 2015 to 2167 in 2025, an increase of 3.5 times. However, its growth rate was significantly lower than that of Class B.

3.2. Quantitative measurement of research attention migration

To measure the relative rise and fall of different drivers more precisely, this study introduced two key metrics: the B/A ratio and the C/(A+B) ratio. Figures 3 and 4 show the changes in both ratios from 2015 to 2025.

Figure 2. The annual variation curve of B/A

Note: B/A ration indicates: how many times more attention architecture gets compared with process; C/ (A+B) indicates: the share of new paradigms relative to traditional drivers)

DOI: 10.54254/2755-2721/2026.GL36151

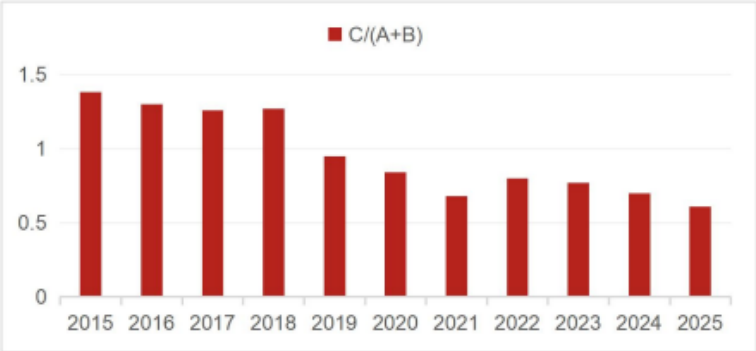

Figure 3. The annual variation curve of C/(A+B)

Note: B/A ration indicates: how many times more attention architecture gets compared with process; C/ (A+B) indicates: the share of new paradigms relative to traditional drivers)

The B/A ratio reveals a major shift. In 2015, category B papers were about 5.4 times the number of category A papers. By 2025, that ratio had reached 35.8 to 1. Across 11 years, It increased by almost seven times and the trend shows a significant overall increase. By the end of the study period, for every paper on process scaling, there were more than 35 on architecture innovation. Architecture had therefore moved from an "important complement" to the predominant research focus.

The C/(A+B) ratio reveals a different and interesting pattern. It fell year by year from 1.38 in 2015 to 0.61 in 2025. Even though the absolute number of category C papers kept rising, their share relative to the combined total of A and B shrank over time. This indicates that the growth rate of academic attention to advanced packaging and new paradigms lagged behind that of the mainstream process and architecture. New paradigms are a meaningful incremental contributor, but they have not become the new mainstream that replaces the traditional paths.

3.3. Core conclusions drawn from the quantitative analysis

Based on the data above, this study points to three main findings: Process-driven research has basically hit a saturation point. The long-term flat trend in category A papers shows that, in terms of academic output, the model of advancing technology solely by shrinking transistors has run into a ceiling. This does not mean process innovation has stopped; rather, the data indicate that progress at the technological level is no longer the primary driving force for academic attention or industrial performance improvement. Instead, it has now become an indispensable fundamental element.

Furthermore, architecture has established an irreversible dominant position. The steady, unidirectional surge in the B/A ratio offers quantitative backing for Hennessy and Patterson's claim about a "new golden age for architecture" [4]. The data show that in the post-Moore era, the main engine of microprocessor progress has shifted from "More Moore" to "More than Moore" in architecture. The driving force behind this transformation is the understanding that has emerged in academia and industry that the most promising method for enhancing processor performance lies in optimizing systems and microarchitectures.

Finally, new paradigm drivers serve as a steady complement, not a replacement. The absolute rise in category C papers is real and should be acknowledged, but the steady decline in its relative share suggests that packaging and new paradigm innovations are still in an ecosystem-building phase. Their trajectory looks more like a long, slow build-up than a short-term breakout.

DOI: 10.54254/2755-2721/2026.GL36151

4. Industry case verification and development implications

4.1. Industrial cases of architecture & chiplet innovation

The above bibliometric analysis reveals the shift in research directions within the academic community. This is not an isolated academic phenomenon but a result that aligns with industry development. The following text demonstrates through two cases examined from different perspectives that in the post-Moore's Law era, architecture and packaging are gradually becoming the main driving forces.

To begin with, DSA has emerged widely. Google first deployed tensor processing units (TPUs) in 2015, marking the transition of DSA from an academic concept to large-scale commercial use [9]. Since then, specialized accelerators for deep learning inference and training have experienced explosive growth, covering both the cloud (such as NVIDIA's H100 Transformer Engine) and the edge (such as Apple's neural engine). Dally et al. pointed out that DSA, through custom hardware for specific computing patterns, can achieve energy efficiency gains of several times at the same node [10]. The performance gains are far greater than what could be achieved solely through process node changes. This industry trend confirms the rapid growth of B-class papers in this field.

In addition, Chip-level technology is moving from concept to mainstream. In 2017, AMD launched the EPYC processor based on the Infinity Fabric interconnection, proving for the first time the commercial feasibility of chip-level architecture in server chips. Since then, Intel has expanded chip-level technology from CPUs to GPUs and FPGAs through EMIB and Foveros technologies, such as products like Ponte Vecchio and Meteor Lake [11]. Naffziger et al. pointed out that chip-level technology is not only a cost optimization method, but also a revolution in architecture [12]. Different functional modules can adopt the optimal process node respectively. This trend reflects the continuous growth in advanced packaging observed in C-class papers, and explains why chiplet architecture research in B-class papers has become popular.

4.2. Multi-driven industrial development strategies

By combining quantitative data with industry cases, this study shows the current development status of microprocessor technology in the post-Moore era: dominated by architectural innovation, and driven by multiple factors. Architectural innovation as the core engine means that it has established this position as the primary driver of performance. "Multiple driving factors" indicate that the relationship among process, architecture, and packaging is being reshaped. The role of process technology is to shrink rather than disappear; it merely shifts from being the leader to becoming a foundational platform that supports architectural and packaging innovations. Based on the above analysis, this study offers the following insights for the industry:

For enterprises, they should prioritize architectural design and advanced packaging capabilities, and view process technology as an enabling platform rather than the only source of competition. The standardization of the chip-level ecosystem and IP reuse will become new competitive battlegrounds. For research institutions, pursuing next-generation process nodes for device research is difficult to achieve high-impact results. Cross-layer innovation integrating architecture, process, and algorithms is a more promising path to breakthroughs. For policymakers, strategic support for the semiconductor industry must go beyond pursuing advanced wafer fabrication lines. A more systematic system is needed, covering architectural design toolchains, chip-level standard ecosystems, and advanced packaging supply chains.

DOI: 10.54254/2755-2721/2026.GL36151

5. Conclusion

In summary, this study is based on top conference papers from the IEEE Xplore database for 2015-2025. It uses bibliometric methods to quantify the driving forces behind post-Moore microprocessor technology. The research divides technological innovation into three categories: process-driven (A), architecture-driven (B), and advanced packaging/new paradigm-driven (C). Through the analysis of the data, the following conclusions are drawn:

In the first place, the development of process miniaturization has entered a plateau. The research paradigm that solely relies on the reduction of transistors has reached a saturation point in terms of academic output. In addition, architectural innovation has become the absolute main driving force in the post-Moore's Law era. lastly, advanced packaging technology and new paradigms are important factors driving progress, but they have not yet become the mainstream trend.

This study has the following limitations: the search formula relies on title keyword matching, which may omit some related papers with ambiguous titles. Meanwhile, the data only comes from the IEEE Xplore database and does not cover other important publishing platforms. Future research can combine full-text keyword analysis and cross-validation of multiple databases to further deepen the understanding of the new driving forces for technological development in the post-Moore's Law era.

References

[1] Moore, G. E. (2006). Cramming more components onto integrated circuits, reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff. *IEEE Solid-State Circuits Society Newsletter, 11*(3), 33-35.

[2] Waldrop, M. M. (2016). The chips are down for Moore's law. *Nature, 530*(7589), 144–147. https://doi.org/10.1038/530144a

[3] Theis, T. N., & Wong, H. S. P. (2017). The end of Moore's law: A new beginning for information technology. *Computing in Science & Engineering, 19*(2), 41-50.

[4] Hennessy, J. L., & Patterson, D. A. (2019). A new golden age for computer architecture. *Communications of the ACM, 62*(2), 48-60.

[5] Shalf, J. (2023). The future of computing beyond Moore's Law. In *Feynman Lectures on Computation* (pp. 311-332). CRC Press.

[6] Bornmann, L., & Mutz, R. (2015). Growth rates of modern science: A bibliometric analysis based on the number of publications and cited references. *Journal of the Association for Information Science and Technology, 66*(11), 2215-2222.

[7] Mentioned, I. (2006). The history and meaning of the journal impact factor.

[8] IEEE. (2024). *International roadmap for devices and systems (IRDS™) 2024 edition*. https://irds.ieee.org/editions/irds2024/

[9] Jouppi, N. P., Young, C., Patil, N., Patterson, D., Agrawal, G., Bajwa, R., ... & Yoon, D. H. (2017, June). In-datacenter performance analysis of a tensor processing unit. In *Proceedings of the 44th annual international symposium on computer architecture* (pp. 1-12).

[10] Dally, W. J., Turakhia, Y., & Han, S. (2020). Domain-specific hardware accelerators. *Communications of the ACM, 63*(7), 48-57.

[11] Mahajan, R., Sankman, R., Patel, N., Kim, D. W., Aygun, K., Qian, Z., ... & Mallik, D. (2016, May). Embedded multi-die interconnect bridge (EMIB)--a high density, high bandwidth packaging interconnect. In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)* (pp. 557-565). IEEE.

[12] Naffziger, S., Beck, N., Burd, T., Lepak, K., Loh, G. H., Subramony, M., & White, S. (2021, June). Pioneering chiplet technology and design for the amd epyc™ and ryzen™ processor families: Industrial product. In *2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA)* (pp. 57-70). IEEE.