

Design and Simulation of an Intelligent 48V DC Power Distribution and Management System

Xingchen Jiang

*College of Electrical and Power Engineering, Hohai University, Nanjing, China
2305020214@hhu.edu.cn*

Abstract. With the increasing use of 48V microgrids in telecommunication facilities, RVs and distributed energy storage systems, it is necessary to build an efficient dynamic load scheduling system and strong battery protection circuit at the same time. Based on the above analysis, a complete design and evaluation of the 48V direct current intelligent power distribution topology are proposed in this paper. A close connection has been established between the MCU and BMS; thus, both can be dynamically turned off quickly and high-speed fault isolation can also be carried out. A basic part of this research is to study how different gate-drive forms affect the operation of solid-state power switches (MOSFETs). According to the simulation results, using low-side N-channel MOSFET switches with fast-recovery flyback diodes and optimised RC snubber networks can effectively reduce high-voltage inductive transients. Thus, this MCU-centred architecture will be more functionally stable, scalable and thermally safe for current low-voltage DC energy control systems.

Keywords: power distribution, solid-state relay, low-side MOSFET, dynamic load shedding, transient suppression

1. Introduction

1.1. Background and problem statement

Electromechanical relays have long dominated low-voltage DC power routing applications due to their straightforward contact mechanics and galvanically isolated operational properties. However, as contemporary power distribution evolves toward "Smart Grid" paradigms, traditional mechanical switching elements struggle with limited switching speeds, contact arcing, high electromagnetic interference (EMI), and degradation under frequent Pulse Width Modulation (PWM) cycles.

While transitioning to a 48V nominal DC bus improves overall transfer efficiency, it introduces significant stress on semiconductor switches. Inductive components—such as cooling fans, refrigeration compressors, and auxiliary motors—store inductive energy that manifests as large voltage spikes upon turn-off. Without precise microcontroller intervention and BMS integration, unmitigated transient overvoltages and thermal runaway can cause catastrophic semiconductor failures.

To address these limitations, a MCU-centred 48V DC smart power distribution architecture is proposed. The overall system architecture, incorporating the central power bus, BMS coupling,

MCU control unit, and solid-state switching channels, is illustrated in Figure 1.

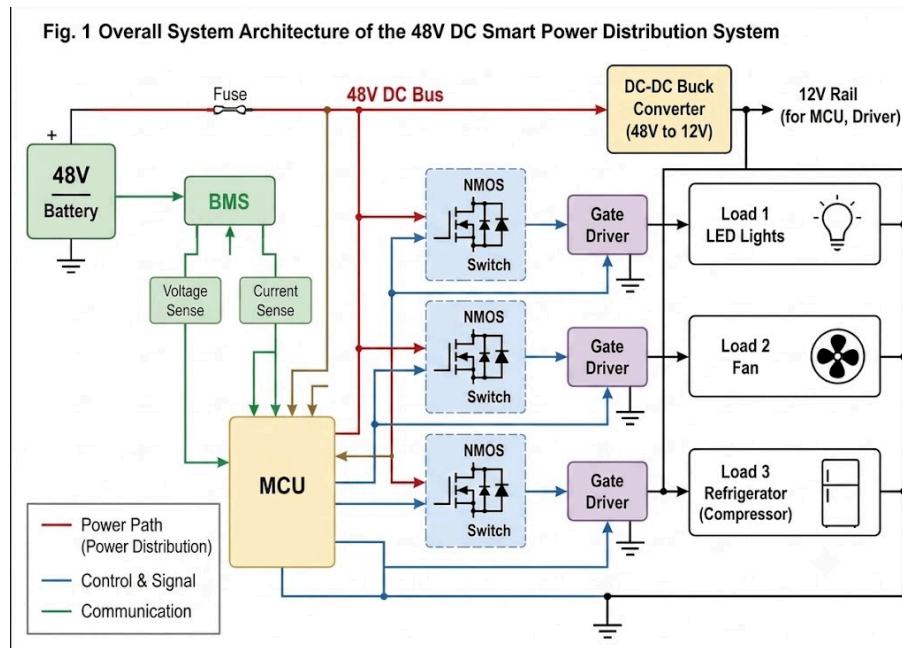


Figure 1. Overall system architecture of the 48V DC smart power distribution system

1.2. Research objectives

In this paper, a fully solid-state power management unit has been designed to meet the following three main engineering performance requirements: conduction efficiency optimisation, minimising ohmic power losses in all power switching branches.

Conduction Efficiency Optimization: Minimizing ohmic power losses ($I^2 R_{DS(on)}$) across all power switching branches.

Active protection means: Add real-time Transient Voltage Suppression (TVS) and Software-Configurable Under-Voltage Lockout (UVLO).

Adaptive Load Shedding Logic: Programming the MCU to continuously calculate the battery state-of-charge (SoC) parameters and cut off the non-critical branches automatically when the voltage is low.

1.3. Literature review & related work

With the development of low-voltage DC (LVDC) distribution systems in power electronics, many studies have been conducted. Elsayed et al. [1] showed that removing redundant AC-DC and DC-AC conversion links in residential microgrids can improve total system energy efficiency by about 5% to 10%. Among all the candidate DC bus voltages, the 48V level has become a widely accepted standard; it is also regulated by the EMerge Alliance and IEEE 2030 series 10%, 25%. Based on Justo et al. [2] and Kumar et al. [3], the boundary is chosen as a good one; it works safely under the extra-low-voltage (ELV) safety-compliance limit of 380 V, and there are no strict requirements for high-voltage insulation; at the same time, the resistive losses of copper have been reduced significantly from the previous generation 12V designs. In addition, Prabhakaran et al. [4] pointed out that standardised 48V architectures can greatly improve the integration of renewable energy, especially direct photovoltaic-to-storage coupling 48V, 60V.

Despite the above-mentioned operational efficiency improvements, there are still some engineering problems such as fast circuit protection and inductive load switching in LVDC networks. Traditional electromechanical contactors have an arc during DC interruption because there is no natural zero-crossing point, and they degrade quickly; this was found by Salomonsson et al. [5]. Therefore, solid-state relays (SSRs) and discrete MOSFET power switches have now become the current standard for rapid fault isolation. Miao et al. [6] showed that solid-state circuit breakers (SSCBs) can interrupt fault currents in the range of several tens of nanoseconds, much faster than mechanical devices. However, as pointed out by Park and Candelaria [7], switching unsuppressed inductive loads on a 48V bus will produce huge counter-electromotive force (counter-EMF) transients, and these are easily broken down by semiconductor gate oxides or exceed the drain-source breakdown voltage. To solve the problem of inductive ringing, Chen et al. [8] think that an active snubber network and a fast-clamping flyback diode should be used.

In recent years, research on the control of microgrids based on MCUs has mainly focused on the recovery of the state-of-charge (SoC) and dynamic load shedding. Meng et al. [9] and Lu et al. [10] have shown that coordinating power-handling electronics with real-time Battery Management System (BMS) telemetry can prevent premature battery degradation and system-wide voltage collapse. Based on the above research, in this paper, a low-side N-channel MOSFET topology is used in combination with an embedded MCU logic to build an arc-free, highly efficient, transient-protected 48V smart distribution platform.

2. Comparison of the topological structures of switching devices and gate drivers

The choice of a suitable solid-state switching topology will determine the thermal performance of the system, the complexity of the circuit layout, and the total BOM cost. Three candidate topologies were chosen, shown in Table 1.

Table 1. Comparison of switching topologies for 48V systems

Topology	Device Type	Side	Gate Drive Req.	RDS (on)	Efficiency	Complexity	Remarks
PMOS High-Side	P-Channel	High	Simple (Gate–GND)	High	★☆☆ (Low)	Low	Easy to drive; high 48V loss
NMOS High-Side	N-Channel	High	Complex (>48V boost)	Low	★★★ (High)	High	Efficient; requires charge pump
NMOS Low-Side (Chosen)	N-Channel	Low	Simple (Gate–12V)	Low	★★★ (High)	Low	Optimal balance of loss & control

2.1. High-side p-channel MOSFET (PMOS) switches

High-side PMOS switches can reduce the number of control signals; that is, pulling the gate node to Ground will turn on the device. However, at a 48V baseline, the internal drain-source resistance ($R_{DS(on)}$) of available PMOS devices is much higher than that of N-channel devices with the same die size. Furthermore, the maximum rating of a typical power MOSFET gate oxide layer is $V_{GS} = \pm 20V$. When you apply 0V to the PMOS gate and leave it at 48V for the source, you will create an absolute differential voltage of 48V immediately destroying the gate oxide layer without using a voltage divider level-shifting circuit.

2.2. High-side N-channel MOSFET (NMOS) switches

NMOS switches have good conduction performance and a small $R_{DS(on)}$ value. However, to operate an NMOS device on the high side, the gate potential must be higher than the drain supply voltage (e.g., $V_{gate} \approx 58V - 60V$ for a $48V$ source) to guarantee full channel enhancement.

Generating this floating bias voltage requires dedicated bootstrap networks or charge-pump ICs, which increases component count, layout footprint, and system cost.

2.3. Low-side N-channel MOSFET (NMOS) switching architecture

In order to achieve the highest possible overall operational efficiency and keep the control circuit simple, a low-side NMOS switching configuration has been used for Load 1 (Lighting), Load 2 (Ventilation Fan), and Load 3 (Refrigeration Compressor). Positioned at the end of the load return path and in parallel with the system Ground, the MOSFET gate is directly driven by a ground-referenced gate driver IC that receives standard MCU logic levels.

3. System architecture and hardware logic integration

3.1. Central power bus and auxiliary conversion

The DC bus is a 215-292 character long. To reduce the voltage for the MCU logic rails and gate driver ICs, a buck converter with a high step-down ratio has been added. The output voltage is controlled by the standard buck formula: $48V$

$$V_{out} = D \times V_{in} \quad (1)$$

The switching duty cycle is denoted by the symbol. The selection of a buck regulator should be able to handle input surges of up to cope with transients from float-charging voltages in solar controllers or AC-DC rectifiers at the front end.

3.2. Battery management system (BMS) coupling

The BMS interface is constantly measuring the battery voltage, pack temperature and individual cell state-of-charge, etc., and reports the diagnostic status to the MCU:

UVLO, when the battery bus voltage is less than 15 cells of fully discharged LiFePO₄ batteries ($42V$), will make the MCU change its working mode and send a global disable command to all the gate driver stages.

Over-Current and Short-Circuit Protection: The MCU uses a high-side current-sense amplifier to measure the bus current. Voltage drop anomalies will trigger an interrupt routine that will immediately cut off non-critical operational loads (Load 1 and Load 2) within microseconds.

The low-side NMOS switching channel is integrated with a flyback diode and an RC snubber network (Figure 2).

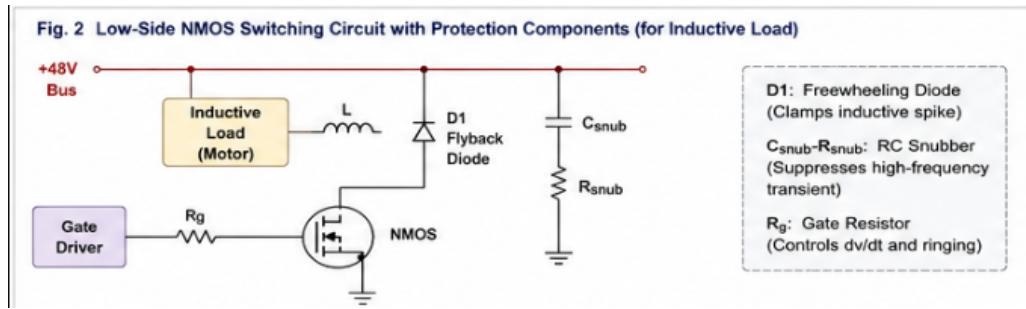


Figure 2. Low-side NMOS switching circuit with protection components(for inductive load)

4. Circuit simulations and empirical results

4.1. Inductive transient suppression

Based on the load 2 (Fan motor) and Load 3 (Compressor) inductive loads, a transient voltage risk was modelled with them. The basic voltage-current characteristic of an inductor is shown in the figure above.

$$v(t) = L \frac{di(t)}{dt} \quad (2)$$

when the low-side MOSFET is turned off suddenly, a large negative current gradient will be generated ($\frac{di}{dt} \ll 0$), and a large positive inductive flyback spike will appear at the drain terminal. Therefore, integrating a freewheeling diode across the inductive load is highly vital.

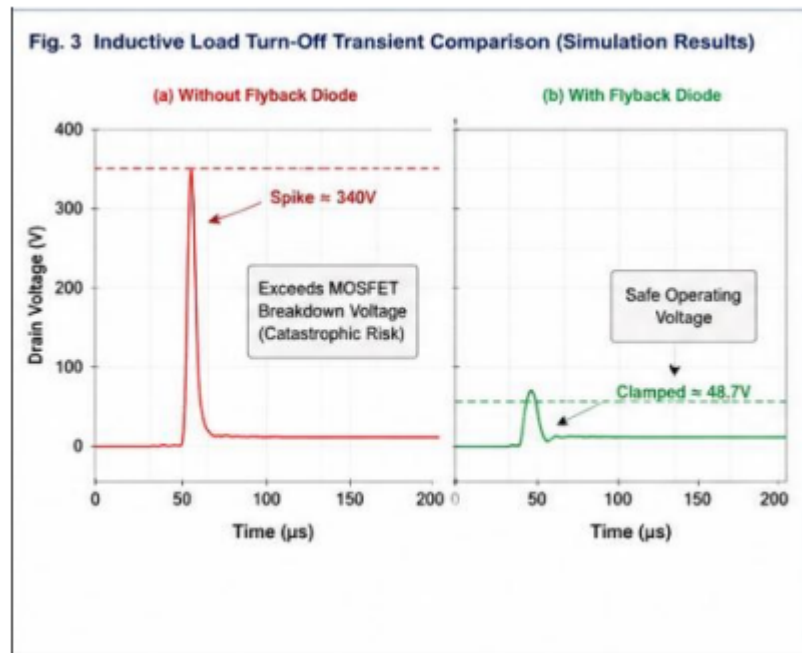


Figure 3. Inductive load turn-off transient comparison(simulation results)

The flyback diode effectively suppresses the inductive spike and clamps the drain voltage to 48.7V, as shown in Figure 3.

Baseline Simulation (Unprotected): Switching off an inductive load without freewheeling protection yielded a voltage transient peaking at approximately 340V. This far exceeds standard semiconductor breakdown thresholds, causing device failure.

With the addition of an ultra-fast recovery diode on both ends of the inductive load, we can effectively suppress the voltage spike (48.7V) caused by switching and release the stored magnetic energy in a safe way.

4.2. Gate drive resistor (R_g) tuning

The gate series resistance (R_g) was tuned across a range of 0Ω to $1k\Omega$ at a PWM switching frequency of $20kHz$:

Extremely Low Resistance ($R_g \rightarrow 0\Omega$): Rapid gate charge accumulation ($\frac{dv}{dt}$) caused significant high-frequency ringing and severe electromagnetic interference (EMI).

Excessive Resistance ($R_g \rightarrow 1k\Omega$): The MOSFET transition time in the linear region has been extended, and as a result, switching losses have increased greatly (P_{sw}) and the temperature of the device has risen.

Optimal Balance: A value between 10Ω and 47Ω provides a sharp switching transition without causing too much EMI or parasitic ringing.

A gate resistance (R_g) between 10Ω and 47Ω achieves an optimal balance between EMI ringing and switching loss, as summarized in Figure 4.

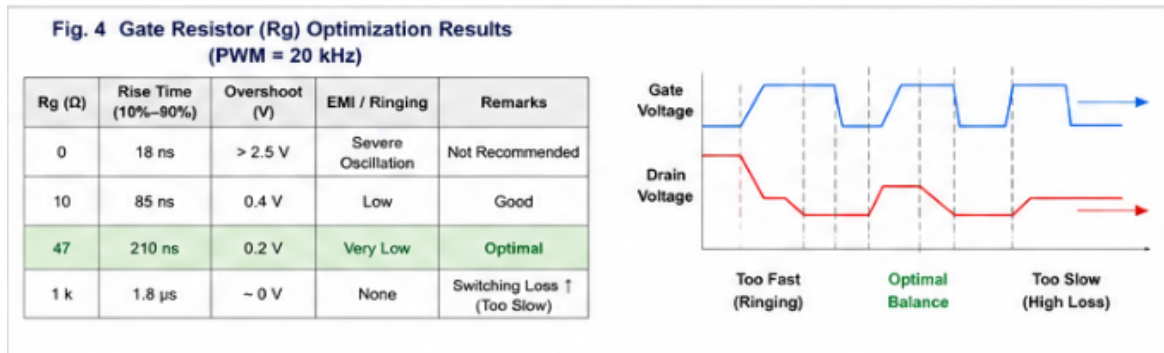


Figure 4. Gate register(R_g) optimization results(PWM=20kHz)

4.3. Thermal loss modeling

The steady-state operating heat generation of Load 3 (Refrigerator) at continuous rating 10A was calculated. The formula for calculating conduction losses is as follows:

$$P_{loss} = rms_2^I \times R_{DS(on)} \quad (3)$$

Choose a low-resistance N-channel MOSFET ($R_{DS(on)} = 5m\Omega$) to meet the following requirements:

$$P_{loss} = (10 \text{ A})^2 \times 0.005 \Omega = 0.5 \text{ W} \quad (4)$$

The calculated conduction loss is only 0.5W, which eliminates the need for an active cooling fan , as illustrated in Figure 5.

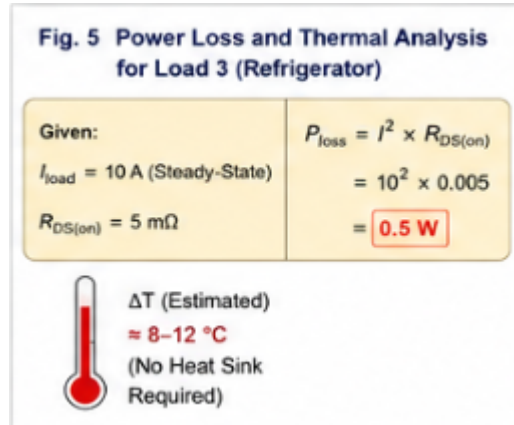


Figure 5. Power loss and thermal analysis for load 3 (refrigerator)

The low-power dissipation is sufficient for passive cooling (copper PCB thermal vias), and there is no need for an active-cooling fan on the distribution board.

5. Control firmware execution strategy

The microcontroller will continuously carry out the task of power health inspection and load-priority control in a loop. The MCU continuously monitors bus voltage and BMS telemetry to execute adaptive load shedding , as depicted in Figure 6.

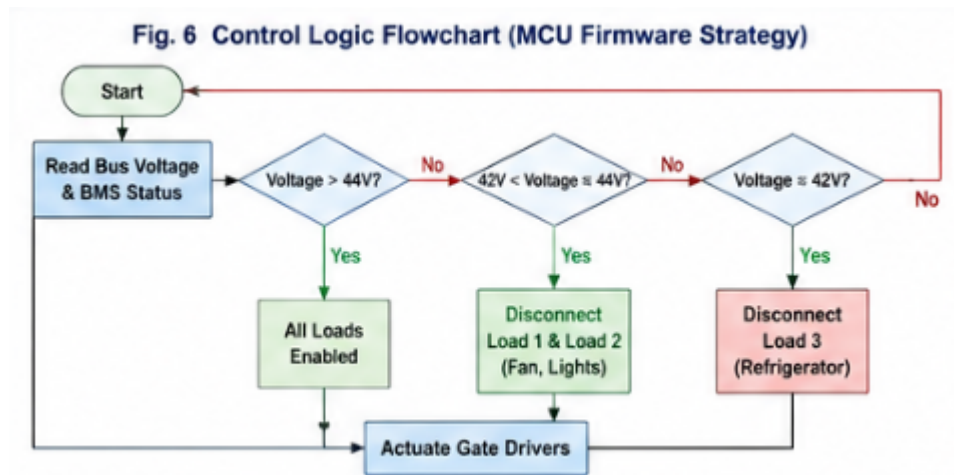


Figure 6. Control logic flowchart(MCU firmware strategy)

6. Conclusions and future research extensions

6.1. Conclusions

This paper shows that the MCU-controlled low-side NMOS switching control architecture of the DC intelligent power management system in this paper is good for thermal performance, operation and design 48V. Software-defined protective logic has more flexible configuration options than traditional hardware fuses and thermal breakers. Simulation results show that ultra-fast flyback diodes and properly tuned gate resistors are needed to suppress voltage transients when driving inductive motor loads.

6.2. Future research extensions

To further improve performance, future versions will be added with the following improvements:

1. Shunt-based current monitoring; add low-side current shunts($1m\Omega$)to each output channel to be able to perform real-time current telemetry and soft over-current tripping.
2. PWM soft-start Integration: Add digital soft-start procedures to the MCU firmware to manage motor inrush current during the first few cycles of compressor start-up.
3. Add the RS485 Modbus or CAN-bus protocol to make it possible for the industrial communication integration system to work well with off-grid hybrid inverters and MPPT solar charge controllers.

References

- [1] Elsayed, A. A., Mohamed, A., & Mohammed, O. A. (2015). DC microgrids and distribution systems: An overview. *Electric Power Systems Research*, 119, 407–417.
- [2] Justo, J. J., Mwasilu, F., Lee, J., & Jung, J. W. (2014). AC-DC microgrids overview: Architectural topologies, control strategies and resilience. *Renewable and Sustainable Energy Reviews*, 35, 332–349.
- [3] Kumar, D., Zare, F., & Ghosh, A. (2017). DC microgrid technology: System architectures, low-voltage DC breaker topologies, and power quality challenges. *IEEE Access*, 5, 12246–12256.
- [4] Prabhakaran, P., Goyal, Y., & Agarwal, V. (2018). Novel communication-less control strategy for coherent power sharing in a hybrid DC microgrid. *IEEE Transactions on Power Electronics*, 33(4), 3046–3057.
- [5] Salomonsson, J., Söder, L., & Sannino, A. (2009). Protection of low-voltage DC microgrids. *IEEE Transactions on Power Delivery*, 24(3), 1045–1053.
- [6] Miao, Z., Chin, K. A. A., & Yeoh, S. S. (2021). Solid-state circuit breaker protection for DC microgrids: Principles, topologies, and future trends. *IEEE Open Journal of Power Electronics*, 2, 520–537.
- [7] Park, J. D., & Candelaria, J. (2013). Fault detection and isolation in low-voltage DC bus microgrid system. *IEEE Transactions on Power Delivery*, 28(2), 779–787.
- [8] Chen, X., Li, C., & Sun, K. (2019). Design and evaluation of RC snubber and flyback clamping circuits for low-voltage power MOSFETs. *IEEE Transactions on Industrial Electronics*, 66(8), 6112–6121.
- [9] Meng, L., Shafiee, Q., Trecate, G. F., Karimi, H., Valencia, D. F., Guerrero, J. M., & Asuncion, E. A. A. (2017). Review on control of DC microgrids and DC microgrid clusters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(3), 1223–1243.
- [10] Lu, X., Sun, K., Guerrero, J. M., Vasquez, J. C., & Huang, L. (2014). State-of-charge balance control of distributed energy storage systems in DC microgrids. *IEEE Transactions on Industrial Electronics*, 61(6), 2804–2815.