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Carrier Transport and Switching Characteristics in Silicon Logic Devices

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Abstract. As the dimensions of silicon-based devices continue to shrink, the efficient transport of charge carriers has become a key factor determining switching speed and power consumption. This study focuses on the primary carrier transport mechanisms in silicon, drift, diffusion, scattering, and trap capture, and analyses how they interact in miniaturised transistors to influence overall performance. This paper systematically reviews three key parameters, carrier velocity, doping concentration, and interface quality, and evaluates their impact on carrier transport in silicon MOSFETs. Insufficient carrier mobility or excessive interface traps fundamentally limit switching speed and stability. The review further discusses common performance optimisation approaches, such as strained silicon, silicon-germanium channels, and surface passivation techniques as engineering routes to improve charge transport while reducing power consumption. Systematic optimisation of carrier transport can significantly reduce switching times and cut power consumption.

Keywords: Carrier transport, Silicon MOSFET, Switching characteristics, Carrier mobility, Interface traps

1. Introduction

Silicon-based logic devices lie at the heart of modern integrated circuits, and their performance gains largely depend on the precise control of charge carriers. As transistors shrink into the nanoscale regime, short-channel effects, strong interface scattering, and velocity saturation disrupt normal carrier transport, slowing device switching and significantly increasing power consumption [1]. This has long been a key bottleneck in advanced device scaling, and fundamental transport analysis shows that mobility degradation is one of the main factors limiting performance in short-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), as it directly reduces the ability of carriers to support drift current in the channel [2].

Existing studies have shown that carrier mobility, scattering mechanisms, and temperature dependence directly affect the on-state and off-state currents of MOSFETs. Yet, the coupled influence of these factors at the nanoscale has not been fully and systematically analyzed [2]. A 2019 study in Nature Communications also noted that nanoscale confinement significantly alters carrier transport, but the specific coupling mechanism remains unclear [3].

Therefore, exploring how electrons and holes are transported in silicon channels carries both theoretical and engineering value. It investigates carrier transport models, focusing on two key

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questions: how carrier transport determines the switching performance of macroscopic devices, and how materials and structures can be optimised to enhance device efficiency. The research can help designers better understand the physical limits of silicon logic devices and provide practical guidance for optimizing processes and improving the performance of advanced devices such as Fin Field-Effect Transistors (FinFETs) and nanosheet transistors.

2. Introduction to carrier transport in silicon semiconductors

2.1. Core research directions

As silicon devices have continued to scale down, research on carrier transport has also evolved. Early studies by Shockley focused mainly on drift and diffusion theory, which explained how charge carriers move in semiconductors [4]. Later, researchers realised that smaller devices introduced additional problems that could not be ignored. Takagi et al. showed that surface scattering lowers carrier mobility in MOSFETs and Lundstrom later studied quasi-ballistic transport in short-channel devices [5, 6]. More recent IRDS reports suggest that transport effects are now a major limit to further performance scaling [7].

2.2. Transport properties of electrons and holes

In silicon, electrons and holes do not behave identically in the presence of an electric field. Electrons move through the conduction band, in which the energy varies a steep dispersion relation with momentum, so their response to the field is relatively strong. Holes are located within the valence band, which has a flatter energy dispersion and consists of heavy-hole and light-hole subbands, resulting in less directional transport and higher susceptibility to scattering.

Because of this difference in how they move, room-temperature measurements give mobilities of about 1350 $cm^2\ V^{-1}\ s^{-1}$ for electrons and roughly 450 $cm^2\ V^{-1}\ s^{-1}$ for holes [4]. This gap generally leads to a slowdown in operations and increased power consumption.

2.3. Intrinsic and extrinsic carriers

Intrinsic silicon does not conduct well at room temperature because its free-carrier concentration is low. In practical devices, impurities are therefore deliberately added, a process known as doping. Phosphorus provides extra electrons, producing n-type silicon, while boron introduces holes and produces p-type silicon [8]. However, the doping concentration has a significant effect. Increasing it improves conductivity by supplying more charge carriers, but it also disturbs the crystal lattice, strengthening impurity scattering and reducing carrier mobility [5]. A higher doping level thus involves a trade-off between improved conductivity and reduced carrier mobility.

2.4. Carrier recombination and generation

Carrier recombination occurs when an electron in the conduction band fills a hole in the valence band, removing an electron–hole pair. Generation is the opposite process, where thermal energy creates new electron–hole pairs. In silicon, recombination can occur via radiative, Auger, or defect-assisted Shockley–Read–Hall (SRH) pathways, with SRH usually dominating due to traps and crystal defects.

The dominant sources of off-state leakage in scaled MOSFETs are subthreshold diffusion, gate-induced drain leakage, and band-to-band tunnelling, not slow recombination. Recombination mainly

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affects the turn-off transient tail and the depletion-region leakage component; the latter increases at higher temperatures due to thermal generation through defects [6].

3. Core carrier transport mechanisms and device performance

3.1. Drift, diffusion, and leakage current

Carriers in silicon move mainly through drift and diffusion. An electric field drives drift and dominates when the transistor is in the on state, with its strength strongly dependent on carrier mobility. At low fields, carrier velocity increases roughly linearly with the field, but this relationship becomes less accurate in very short channels under strong electric fields [9].

Diffusion, on the other hand, arises from non-uniform carrier concentration, where carriers move from regions of higher density to lower density. In MOSFETs, this mechanism becomes more important in the subthreshold region, where the device is not fully turned on.

In this regime, diffusion together with weak residual conduction paths leads to a small but persistent leakage current even in the off state. As device dimensions shrink, this leakage becomes more significant and can contribute noticeably to total power consumption, making its control a key concern in low-power design [7, 9]. This inconsistency has prompted a re-examination of how these two mechanisms contribute to leakage current in scaled devices.

3.2. Scattering, temperature, and scaling effects

Carrier mobility in silicon is not fixed, as it varies with the frequency of carrier scattering during transport. The main sources of this disturbance are lattice scattering from atomic vibrations, ionized-impurity scattering from dopant atoms, and interface scattering at the $Si–SiO_2$ interface [4, 5, 7].

Lattice scattering becomes stronger when the temperature increases, because lattice vibrations are more intense and carriers are interrupted more frequently. Ionized impurity scattering depends more on how heavily the material is doped, where charged dopants act as fixed electrostatic disturbances along the carrier path. Interface scattering becomes more important when devices are scaled down, since carriers are pushed closer to the oxide boundary, where surface roughness and trapped charges start to have a stronger effect.

When device sizes reach the nanometre scale, transport behaviour begins to deviate from the bulk silicon picture. Quantum confinement begins to affect carrier distribution across the channel. Unlike the classical picture where the carrier concentration peaks at the $Si–SiO_2$ interface, confinement pushes the wavefunction peak away from the interface into the substrate [10]. While this shift can partly mitigate direct interface scattering, it also increases the effective oxide thickness, reducing gate control.

At the same time, the reduction in channel length weakens the gate's electrostatic control. As a result, small local variations in charge or geometry have a larger impact on device behaviour. Classical mobility-based models, therefore, become less accurate and more complete models that include both quantum effects and interface scattering are needed.

3.3. Transport limits and performance dependence

At high electric fields, the carrier velocity in silicon no longer increases. It gradually levels off at a value known as the saturation velocity, which is about 1×10^7 cm/s for electrons in silicon [11]. In short-channel devices, this tends to occur earlier because the electric field becomes very strong over

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a short distance. Once this takes places, increasing the voltage further has much less effect on the current, effectively capping carrier transport [12].

This links directly to switching behaviour. Transistor operation essentially involves charging and discharging the gate and channel capacitances, so the speed depends on how quickly carriers can move through the channel. Higher mobility allows this process to take place faster, since carriers respond more efficiently to changes in gate voltage. With reduced mobility, carrier motion slows, and the time required for full charge and discharge increases, reducing switching speed.

In practical Complementary Metal-Oxide-Semiconductor (CMOS) devices, strain engineering is often used to mitigate this limitation. Experimental results from strained 90 nm CMOS devices show an increase in effective electron mobility, extracted from transconductance and Id–Vg measurements [13]. This increase leads to higher drive current and shorter charging and discharging times, so the effect shows up both in transport behaviour and in circuit-level performance.

Temperature adds another layer to this behaviour. As temperature increases, lattice vibrations become stronger, and scattering becomes more frequent, reducing mobility. At the same time, thermal excitation produces more free carriers, increasing leakage current even when the device is off. These two effects are linked in operation: higher power dissipation raises temperature, further reducing transport efficiency and increasing leakage, forming a feedback loop that becomes more pronounced in real devices [14].

4. Optimisation technologies for carrier transport

4.1. Crystal band engineering and strain-based mobility enhancement

One of the fundamental limitations in silicon-based devices is the relatively low carrier mobility, which restricts how efficiently carriers respond to an applied electric field. This limitation arises from band-structure properties and scattering processes within the silicon lattice, making mobility improvement an important target in device engineering.

A widely used solution is strain engineering, which modifies the channel's crystal lattice to alter its electronic band structure. By introducing either tensile or compressive strain, the energy band alignment and effective carrier mass can be altered, thereby reducing the scattering probability and improving carrier transport. In CMOS technology, tensile strain is typically applied to nMOS devices to enhance electron mobility, while compressive strain is used for pMOS devices to improve hole mobility. This approach became especially important from around the 90 nm technology node, where further performance improvement was required without relying solely on geometric scaling [15].

Experimental comparisons of strained and unstrained 90 nm CMOS devices show a clear increase in drive current under identical gate-bias conditions. This improvement is accompanied by an increase in the effective electron mobility, as determined from transconductance and Id–Vg measurements, confirming that carrier transport in the channel is directly enhanced [15]. The observed effect is attributed to strain-induced modifications in the silicon band structure and a reduction in intervalley scattering, both of which contribute to improved carrier mobility.

In practical implementation, strain is introduced through several engineering techniques. A common approach is to use SiGe in or around the source and drain regions, which induces strain in the silicon channel via lattice mismatch. This method is widely used because it can be integrated into existing CMOS process flows. Other techniques include embedded SiGe stressors and process-induced strain layers, all aimed at tailoring channel strain without fundamentally altering the device

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architecture [16]. Together, these methods form an important part of modern channel engineering, allowing mobility enhancement through material design rather than continued device scaling.

4.2. Interface and gate engineering

Because interface scattering has such a strong impact, the quality of the Si–SiO_2 boundary becomes critical. Interface passivation is a set of chemical or thermal treatments used to reduce charge-trap states and smooth surface irregularities.

To mitigate this, high-k dielectric and metal-gate engineering are commonly used to improve electrostatic control and reduce interface-trap density. Experimental studies on advanced passivation structures show improved effective mobility and reduced trap-related scattering compared with conventional Si–SiO_2 interfaces, confirming that interface engineering can simultaneously suppress mobility loss and leakage increase [7].

4.3. Novel semiconductor device structures

As traditional planar transistors became harder to scale, the industry began moving towards 3D transistor designs. FinFETs and newer gate-all-around (GAA) nanosheet transistors place the gate around the channel on multiple sides instead of just on top. This gives the gate much better control over the channel.

Better control means less current leakage and weaker short-channel effects, which are major problems in very small transistors. These structures also make it easier to use improved channel materials, such as strained silicon or SiGe, without causing significant stability issues. Because of this, silicon transistors have continued shrinking into the sub-5 nm generation [10].

5. Current challenges and future prospects

5.1. Technical bottlenecks in high-speed/high-integration devices

Even after decades of development, tackling challenges at the sub-5 nm scale remains critical for researchers. Scaling usually improves one aspect of device behaviour while affecting another. Reducing the channel thickness strengthens gate electrostatic control and helps suppress short-channel effects, but it also alters the carrier distribution. Carriers are confined to a narrower potential well, making the precise shape of the confining potential increasingly important. Consequently, device behaviour becomes more sensitive to structural variations such as surface roughness and interface charges. Mobility tends to degrade as channel thickness decreases, despite improved electrostatics.

Device-to-device uniformity becomes harder to maintain at nanoscale dimensions. Random dopant fluctuations and line-edge roughness introduce variations during fabrication, leading to shifts in threshold voltage and changes in carrier mobility even when devices are nominally identical. With transistor counts reaching billions, these variations no longer average out; instead, they manifest as a noticeable spread in performance and a reduction in overall yield. Even minute fabrication-induced differences can cause nominally identical devices to behave differently, and once billions of transistors are integrated on a single chip, such small deviations accumulate and become significant.

Leakage current is also becoming harder to control as chips become more densely packed. A portion of the current flows along unintended paths rather than contributing to useful operation. At

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scale, even this small loss adds up across the entire chip, resulting in wasted power and additional heat.

5.2. Future directions in carrier transport

Research is likely to move in several important directions. As devices continue to shrink, quantum transport effects such as tunnelling and ballistic transport will become increasingly important, requiring new modelling approaches. At the same time, materials beyond silicon, such as 2D materials and other high-mobility channel options, are being explored to push past the speed limits of traditional Si-based devices. Progress will also depend on combining material selection, 3D device design, and thermal management rather than treating them separately to better balance power and performance. In addition, machine learning is increasingly playing a useful role in understanding complex transport behaviour and optimising fabrication processes that are beyond the reach of traditional methods.

6. Conclusion

This paper explores how charge-carrier transport in silicon logic devices affects switching performance. Drift, diffusion, and scattering at the microscopic level strongly determine device behaviour and set fundamental limits on speed and power consumption. Methods such as strain engineering and three-dimensional device structures can improve performance, but they represent mitigation strategies rather than complete solutions.

This study has several limitations. This work focuses primarily on macroscopic transport mechanisms and established experimental results, and does not cover atomistic quantum transport simulations, which are becoming increasingly important for very advanced devices. Reliability issues, including long-term degradation, were not examined in detail. Future research will focus more closely on quantum effects and ballistic transport in ultra-short channels, as well as on alternative channel materials beyond silicon. As devices continue to scale down, carrier transport remains a central challenge.

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