Proceedings of CONF-FMCE 2026 Symposium: Artificial Intelligence and Smart Sensing for Mechanical and Electrical Systems
DOI: 10.54254/2755-2721/2026.BA36356

Power Consumption Bottlenecks and Materials Innovation Pathways for Silicon-Based Logic Devices in the Post-Moore Era

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Abstract. As silicon-based CMOS logic devices continue to scale down, problems such as short-channel effects, quantum tunneling, and the subthreshold swing limit are becoming increasingly pronounced. Power consumption has become a key factor affecting chip performance, thermal management, and energy efficiency. This paper presents a systematic literature review to analyze the power consumption mechanisms of silicon-based logic devices and the associated material-level factors. It reviews the major challenges faced by conventional silicon, gate dielectrics, strained silicon, and interconnect materials in low-power applications, with emphasis on potential solutions including high-mobility channel materials, high-k gate dielectrics, heterogeneous integration structures, low-resistance interconnect materials, and high-efficiency thermal management materials. It also discusses opportunities for materials innovation in the post-Moore era. The review indicates that, under advanced process conditions, device-structure optimization alone cannot adequately meet power-control requirements, whereas materials innovation may provide new technological pathways to improve device energy efficiency. Emerging materials, including high-k dielectrics, two-dimensional semiconductors, carbon-based materials, and ferroelectric materials, offer promising opportunities to reduce leakage current, optimize operating voltage, and enhance energy efficiency. This paper provides a theoretical foundation for the design of low-power integrated circuits and semiconductor materials research.

Keywords: silicon-based logic devices, power consumption bottlenecks, short-channel effects, low-power materials, semiconductor materials innovation

1. Introduction

Since the invention of integrated circuits, silicon-based CMOS technology has relied on dimensional scaling to drive exponential growth in computing capability and integration density, supporting the rapid development of mobile devices, artificial intelligence, data centers, and the Internet of Things [1, 2]. In the nanoscale era, transistor gate lengths are approaching physical limits, and gate dielectrics continue to scale down. Short-channel effects and quantum tunneling cause leakage current to rise exponentially, sharply increasing the proportion of static power. Chip power density

DOI: 10.54254/2755-2721/2026.BA36356

has exceeded thermal-dissipation limits, resulting in severe heat generation, shorter battery life, and reduced reliability [3, 4]. Although structural improvements such as FinFETs and gate-all-around (GAA) devices have been applied at advanced nodes, further scaling has made reliability, process complexity, and interface control increasingly challenging. The power-consumption crisis not only constrains the deployment of advanced process technologies but is also a core limitation for global computing infrastructure and portable electronics. In this context, overcoming the intrinsic limitations of silicon through materials science has become a key direction for mitigating the power crisis and sustaining the development of integrated circuits [5, 6].

Knobloch et al. noted that, as CMOS devices scale to nodes below 12 nm, conventional silicon channels experience mobility degradation due to reduced channel thickness and enhanced interface scattering, making it difficult to continue meeting the requirements of low-power logic [7]. Therefore, two-dimensional semiconductors, owing to their atomic-scale thickness and strong gate controllability, are considered promising candidates for future silicon-based low-power devices. However, their application remains limited by issues such as contact resistance, gate-dielectric deposition, and wafer-scale integration. Liu et al. proposed an approach using GeSn alloy and demonstrated that GeSn/Ge vertical gate-all-around nanowire MOSFETs can improve carrier mobility and drive capability. They also successfully realized a GeSn CMOS inverter, validating the potential of GeSn for developing silicon-compatible low-power logic circuits [8].

Using a literature review approach, this paper examines the power consumption problem of silicon-based logic devices from three perspectives: power consumption mechanisms, material-level challenges, and innovative solution pathways. It also discusses development trends in low-power materials and collaborative optimization strategies for the post-Moore era. The aim is to enhance understanding of power-consumption issues in advanced CMOS devices and provide a reference for the development of integrated circuits in the post-Moore era.

2. Power consumption mechanisms and key issues of silicon-based logic devices

2.1. Physical components of power consumption in silicon-based logic devices

The total power consumption of silicon-based CMOS logic devices can generally be divided into dynamic, static, and short-circuit power. Dynamic power consumption mainly arises from the charging and discharging of load capacitance during transistor switching. It is typically related to the switching activity factor, load capacitance, the square of the operating voltage, and operating frequency, and is one of the main sources of power consumption in conventional CMOS circuits [9]. Static power consumption mainly originates from leakage current when the transistor is off, including subthreshold leakage, gate-oxide tunneling leakage, drain-induced barrier lowering (DIBL)-induced leakage, and source-drain junction band-to-band tunneling leakage. As device dimensions continue to shrink and both threshold voltage and gate-dielectric thickness decrease, static power consumption rises significantly in advanced processes, becoming an important factor limiting low-power design [3]. Short-circuit power consumption is generated by transient current when PMOS and NMOS devices are briefly on at the same time during switching in a CMOS inverter or logic gate. Its magnitude is affected by input-signal transition time, load capacitance, supply voltage, and device dimensions [9].

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2.2. Mechanisms of power-consumption degradation in scaled silicon-based logic devices

When MOSFET channel lengths enter the nanoscale regime, short-channel effects become pronounced, and the electrostatic control of the gate over the channel barrier weakens. Drain-induced barrier lowering (DIBL) reduces the off-state barrier height, thereby increasing off-state leakage current [10]. Meanwhile, as the equivalent oxide thickness of the gate dielectric is further reduced, the probability of direct carrier tunneling through the dielectric increases, leading to higher gate-leakage current and limiting the further scaling of conventional SiO_2 gate dielectrics [4]. In addition, conventional MOSFETs are constrained by thermionic-emission mechanisms at room temperature, making it difficult for the subthreshold swing to fall below approximately 60 mV/dec. This prevents further simultaneous reduction of threshold voltage and supply voltage, thereby limiting the development of low-voltage, low-power logic devices.

2.3. Challenges caused by the power crisis in silicon-based logic devices

Higher power consumption raises junction temperature, which in turn degrades carrier mobility, causes threshold-voltage drift, accelerates electromigration in interconnects, and increases device aging, ultimately affecting chip reliability and service life. In high-performance processors and high-density computing chips, the continued rise in power density poses severe challenges for thermal design, creating the so-called "power wall" or "thermal bottleneck." Meanwhile, high power consumption increases energy costs and thermal-management pressure for data centers, communication base stations, and portable electronic devices. This makes the trade-off among process scaling, performance improvement, and power control more acute, prompting a shift from sole reliance on process scaling toward collaborative innovation in device structures, channel materials, interconnect and packaging materials, and system architectures [6].

3. Pathways and progress in low-power materials innovation

3.1. From power-consumption mechanisms in silicon-based logic devices to materials requirements

As CMOS devices continue to scale, power consumption is gradually evolving from a purely circuit-design problem into one constrained by the joint limitations of materials, devices, and interconnects. At advanced nodes, conventional silicon materials are affected by carrier mobility degradation, increased contact resistance, and insufficient heat dissipation, making it difficult to meet low-power requirements. Meanwhile, gate-dielectric scaling increases quantum-tunneling leakage, while reduced interconnect linewidths raise resistance and RC delay, creating greater challenges for chip power consumption [4].

3.2. Established and emerging materials solutions

Mechanisms that worsen power consumption directly translate into stringent material requirements. Gate dielectrics must have a high dielectric constant to achieve a small equivalent oxide thickness (EOT) while maintaining sufficient physical thickness, thereby suppressing tunneling leakage. Channel materials should have high mobility and a low effective carrier mass to provide adequate drive current even at low VDD, and should also have an ultrathin body structure to enhance gate control and suppress short-channel effects. Source-drain contacts and interconnect materials require

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very low resistivity to reduce RC delay and Joule-heating loss. In addition, efficient thermal-management materials are necessary to indirectly reduce power consumption and ensure reliability.

High-k gate dielectrics and metal-gate technology rank among the most mature low-power solutions currently available. Intel's introduction of a high-k/metal-gate structure in its 45 nm process effectively reduced gate leakage current and improved device performance [11]. In terms of channel materials, strained-silicon technology improves transistor drive capability by increasing carrier mobility and has been successfully applied in 90 nm logic processes.

Germanium-based materials, III-V semiconductors, and two-dimensional semiconductors such as MoS_2 offer higher mobility and stronger gate control, and are expected to further reduce operating voltage and power consumption. However, their industrialization remains constrained by contact resistance, manufacturing cost, and process compatibility [12]. At the interconnect level, low-k dielectrics and emerging interconnect metals can reduce parasitic capacitance and interconnect resistance, thereby reducing dynamic power consumption and improving reliability [10, 13]. In summary, materials solutions at various levels of technological maturity are now available. Table 1 summarizes the application directions and main advantages of representative materials

Table 1. Application directions and advantages of representative materials [7, 8, 10-15]

Material Category	Representative Type	Power Type	Key Benefit
High-k gate dielectrics	HfO_2, ZrO_2	Static	Reduces gate leakage; improves gate control
Metal gates	Metal-gate structures	Static	Improves performance; reduces leakage
Strained silicon	Tensile Si, SiGe	Dynamic	Improves carrier mobility
High-mobility channel materials	GeSn, III-V semiconductors	Dynamic	Higher drive current; lower VDD
2D semiconductors	MoS_2, WSe_2, black phosphorus	Dynamic & static	Suppresses short-channel effects
Low-k dielectrics	Low-k dielectrics	Dynamic	Reduces parasitic capacitance
Emerging interconnect metals	Co, Ru, Mo	Dynamic	Lower interconnect delay; better reliability
Thermal-management materials	Thermal interface materials, advanced packaging	Indirect total	Improves heat dissipation
Ferroelectric materials	Negative-capacitance materials	Dynamic	Reduces subthreshold swing
Carbon nanotubes	CNTs	Dynamic & static	High mobility; low power

3.3. Development opportunities in the post-Moore era

In addition to conventional materials optimization, emerging technologies such as negative-capacitance materials, carbon nanotubes, and spintronic materials provide new directions for low-power logic devices. Negative-capacitance field-effect transistors are expected to overcome the

DOI: 10.54254/2755-2721/2026.BA36356

conventional subthreshold-swing limit. Carbon-nanotube transistors have extremely high intrinsic mobility and atomic-scale dimensions, while their quasi-one-dimensional structure can effectively suppress short-channel effects. Hills et al. demonstrated a modern microprocessor built entirely from carbon-nanotube transistors, which can operate at lower voltages and offers significantly better energy efficiency than CMOS nodes of the same generation [14, 15]. Spintronics and novel computing paradigms use spin waves or magnetic-moment switching for information processing, thereby fundamentally reducing dynamic power consumption. Although these technologies still face obstacles to large-scale application, their development provides an important reference for low-power computing in the post-Moore era.

4. Discussion

4.1. Findings

Existing research and industrial cases indicate that materials innovation has become an important approach for alleviating the power-consumption problem of silicon-based logic devices. High-k gate dielectrics and metal-gate technology have successfully reduced gate leakage current; strained silicon has improved carrier mobility; and low-k dielectrics and emerging interconnect metals have mitigated interconnect-delay issues. These achievements show that optimizing material properties can, to a certain extent, overcome the performance limitations of conventional silicon materials and improve device energy efficiency and system reliability [11].

4.2. Challenges

Although emerging materials show promising application prospects, their industrialization still faces many challenges. The fabrication processes for two-dimensional semiconductors, carbon nanotubes, and negative-capacitance materials are not yet mature, and the cost of large-scale production remains high. Compatibility issues between new materials and existing silicon-based manufacturing processes have not been fully resolved. In addition, device uniformity, long-term reliability, and manufacturing yield limit their widespread application in advanced logic chips [12, 14, 15].

4.3. Development trends of low-power materials in the post-Moore era

Future development will place greater emphasis on the collaborative optimization of materials, device structures, and system architectures. In the short term, high-k gate dielectrics, low-k dielectrics, emerging interconnect metals, and efficient thermal-management materials will remain important directions for reducing power consumption. In the medium and long term, new technologies such as two-dimensional semiconductors, GeSn, carbon nanotubes, and negative-capacitance devices are expected to further improve device energy efficiency. As heterogeneous integration, advanced packaging, and novel computing architectures develop, the collaborative application of multiple materials will become a key trend for low-power logic devices in the post-Moore era [6].

5. Conclusion

This paper analyzes the power-consumption problem of silicon-based logic devices from the perspectives of power-consumption mechanisms, material-level challenges, and development pathways for low-power materials. The results indicate that, as CMOS devices continue to scale,

DOI: 10.54254/2755-2721/2026.BA36356

problems including short-channel effects, gate-leakage current, contact resistance, interconnect RC delay, and thermal-management pressure are gradually intensifying, making it more difficult to improve performance and energy efficiency solely through dimensional scaling and structural optimization. At the materials level, high-k gate dielectrics, metal gates, strained silicon, low-k dielectrics, emerging interconnect metals, and high-thermal-conductivity packaging materials have already played important roles in reducing leakage, improving interconnect delay, and enhancing device reliability. Meanwhile, emerging materials such as two-dimensional semiconductors, GeSn, carbon nanotubes, and negative-capacitance materials provide new research directions for post-Moore low-power logic devices. Although these materials still face challenges in large-scale fabrication, process compatibility, and long-term reliability, they have considerable potential to reduce operating voltage, improve carrier transport, and optimize energy efficiency. Overall, mitigating power consumption in silicon-based logic devices requires multi-level collaborative optimization involving materials, device structures, interconnects, packaging, and thermal management. In the future, as heterogeneous integration, advanced packaging, and novel computing architectures develop, low-power materials will play an increasingly important role in improving integrated-circuit energy efficiency and advancing semiconductor technologies in the post-Moore era.

However, the study lack of experimental data and quantitative comparisons means the power-saving effects of different materials in practical applications have not been systematically evaluated. In addition, some emerging materials remain at the research stage, and their industrial prospects are uncertain. Future research can combine experimental validation and device simulation to conduct a more in-depth analysis of the performance advantages of different low-power materials

References

[1] Moore, G. E. (1965). Cramming more components onto integrated circuits. *Electronics, 38*(8), 114-117.

[2] Dennard, R. H., Gaensslen, F. H., Yu, H. N., Rideout, V. L., Bassous, E., & LeBlanc, A. R. (1974). Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of Solid-State Circuits, 9*(5), 256-268. https://doi.org/10.1109/JSSC.1974.1050511

[3] Roy, K., Mukhopadhyay, S., & Mahmoodi-Meimand, H. (2003). Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proceedings of the IEEE, 91*(2), 305-327. https://doi.org/10.1109/JPROC.2002.808156

[4] Frank, D. J., Dennard, R. H., Nowak, E. J., Solomon, P. M., Taur, Y., & Wong, H.-S. P. (2001). Device scaling limits of Si MOSFETs and their application dependencies. *Proceedings of the IEEE, 89*(3), 259-288. https://doi.org/10.1109/5.915374

[5] IEEE International Roadmap for Devices and Systems. (2023). IRDS 2023: Beyond CMOS and emerging materials integration. *IEEE*.

[6] Theis, T. N., & Wong, H.-S. P. (2017). The end of Moore's law: A new beginning for information technology. *Computing in Science & Engineering, 19*(2), 41-50. https://doi.org/10.1109/MCSE.2017.29

[7] Knobloch, T., Selberherr, S., & Grasser, T. (2022). Challenges for nanoscale CMOS logic based on two-dimensional materials. *Nanomaterials, 12*(20), Article 3548. https://doi.org/10.3390/nano12203548

[8] Liu, M., Junk, Y., Han, Y., Yang, D., Bae, J. H., Frauenrath, M., Hartmann, J.-M., Ikonic, Z., Bärwolf, F., Mai, A., Grützmacher, D., Knoch, J., Buca, D., & Zhao, Q.-T. (2023). Vertical GeSn nanowire MOSFETs for CMOS beyond silicon. *Communications Engineering, 2*, Article 7. https://doi.org/10.1038/s44172-023-00059-2

[9] Chandrakasan, A. P., Sheng, S., & Brodersen, R. W. (1992). Low-power CMOS digital design. *IEEE Journal of Solid-State Circuits, 27*(4), 473-484. https://doi.org/10.1109/4.126534

[10] Gall, D. (2020). The search for the most conductive metal for narrow interconnect lines. *Journal of Applied Physics, 127*(5), Article 050901. https://doi.org/10.1063/1.5133671

[11] Mistry, K., Allen, C., Auth, C., Beattie, B., Bergstrom, D., Bost, M., Brazier, M., Buehler, M., Cappellani, A., Chau, R., Choi, C.-H., Ding, G., Fischer, K., Ghani, T., Grover, R., Han, W., Hanken, D., Hattendorf, M., He, J., … Zawadzki, K. (2007). A 45nm logic technology with high-k + metal gate transistors, strained silicon, 9 Cu

DOI: 10.54254/2755-2721/2026.BA36356

interconnect layers, 193nm dry patterning, and 100% Pb-free packaging. *2007 IEEE International Electron Devices Meeting*, 247-250. https://doi.org/10.1109/IEDM.2007.4418914

[12] Das, S., Sebastian, A., Pop, E., McClellan, C. J., Franklin, A. D., Grasser, T., Knobloch, T., Illarionov, Y., Penumatcha, A. V., Appenzeller, J., Chen, Z., Zhu, W., Asselberghs, I., Li, L.-J., Avci, U. E., Bhat, N., Anthopoulos, T. D., & Singh, R. (2021). Transistors based on two-dimensional materials for future integrated circuits. *Nature Electronics, 4*, 786-799. https://doi.org/10.1038/s41928-021-00670-1

[13] Maex, K., Baklanov, M. R., Shamiryan, D., Iacopi, F., Brongersma, S. H., & Yanovitskaya, Z. S. (2003). Low dielectric constant materials for microelectronics. *Journal of Applied Physics, 93*(11), 8793-8841. https://doi.org/10.1063/1.1567460

[14] Salahuddin, S., & Datta, S. (2008). Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Letters, 8*(2), 405-410. https://doi.org/10.1021/nl071804g

[15] Hills, G., Lau, C., Wright, A., Fuller, S., Bishop, M. D., Srimani, T., Kanhaiya, P., Ho, R., Amer, A., Stein, Y., Murphy, D., Arvind, Chandrakasan, A., & Shulaker, M. M. (2019). Modern microprocessor built from complementary carbon nanotube transistors. *Nature, 572*, 595-602. https://doi.org/10.1038/s41586-019-1493-8