Proceedings of CONF-FMCE 2026 Symposium: Smart City and Infrastructure Engineering
DOI: 10.54254/2755-2721/2026.CH36969

A Fast Transient Electrothermal Network Model for Thermoelectric–Microchannel Hybrid Hotspot Cooling

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Abstract. A fast transient electrothermal network model is developed for thermoelectric–microchannel (TEC–MC) hybrid hotspot cooling, where full three-dimensional multiphysics simulations are computationally prohibitive under time-varying thermal loads. Based on a previously established steady-state thermal-resistance network, heat-conduction and convection paths are represented by thermal resistances, while thermal energy storage in the chip, ceramic substrates, electrodes, thermoelectric legs, and microchannel heat sink is represented by thermal capacitances. Chip heat generation, Joule heating, and Peltier heat are introduced as independent or temperature-controlled heat sources. To resolve the temperature gradient within the thermoelectric legs and the time delay associated with the propagation of volumetric Joule heat toward the cold side, the thermoelectric legs are discretized into 20 layers. The model is implemented in MATLAB/Simulink and validated against both three-dimensional COMSOL simulations and experimental measurements. Under heat-load and current pulse conditions, the maximum relative deviations from the three-dimensional simulations are 0.99% and 0.78%, respectively, while the maximum deviation from the experimental results is 1.61%. For a transient sweep comprising 71 operating points, the reduced-order network model requires approximately 4 s, whereas the corresponding three-dimensional simulations require approximately 20 h, yielding a computational speedup of more than three orders of magnitude. The proposed model captures hotspot spreading, thermoelectric coupling, and microchannel heat rejection, and provides an efficient system-level tool for transient analysis and control-oriented design of TEC–MC integrated cooling systems.

Keywords: thermoelectric cooling, microchannel cooling, hotspot thermal management, transient modeling, electrothermal network

1. Introduction

With the continuing increase in power density in high-performance computing, radio-frequency electronics, and power electronic devices, the local heat flux at chip-surface hotspots can be substantially higher than the chip-averaged heat flux. In contrast to steady-state power dissipation, task switching, load surges, and pulsed operating modes can introduce rapid thermal-load fluctuations. Effective hotspot thermal management therefore requires not only sufficient steady-state heat-rejection capability but also a fast transient thermal response.

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DOI: 10.54254/2755-2721/2026.CH36969

Thermoelectric coolers (TECs) enable rapid, solid-state, and actively controllable cooling through the electrically driven Peltier effect; however, the hot side must promptly reject both the pumped heat and the internally generated Joule heat. Integrating a TEC with a microchannel heat sink having a high heat-transfer coefficient combines the fast controllability of thermoelectric cooling with the strong heat-rejection capability of microchannels, making the hybrid configuration attractive for active thermal regulation of hotspots in high-heat-flux chips [1].

Existing studies of thermoelectric–microchannel systems have primarily relied on experiments, three-dimensional Multiphysics simulations, or simplified models. Experiments capture realistic operating behavior but are costly and limited in parameter space. Three-dimensional models can simultaneously resolve electrical fields, thermoelectric coupling, conjugate heat transfer, and fluid flow, but their computational cost becomes prohibitive for long-duration transient simulations, parametric sweeps, and iterative controller development [2]. Existing transient reduced-order models for thermoelectric devices have mainly focused on individual TECs and have not fully addressed the system-level coupling among lateral hotspot spreading in the chip, interfacial thermal resistance, and the thermal boundary condition imposed by the microchannel heat sink. A system-level transient model that balances physical fidelity, predictive accuracy, and computational efficiency is therefore needed.

This study develops a transient equivalent thermal-resistance network model for a thermoelectric–microchannel integrated cooling system subjected to rapid variations in chip heat load and TEC input current. The model is established on the basis of an existing steady-state thermal-resistance network and is validated against both three-dimensional multiphysics simulations and experiments. The main contributions are as follows: (1) a system-level transient network is developed to represent hotspot spreading, thermoelectric cooling, and microchannel heat rejection within a unified framework; (2) conduction, convection, the Peltier effect, Joule heating, and thermal energy storage are represented consistently; (3) the thermoelectric legs are discretized into distributed thermal-resistance–capacitance–heat-source elements along their thickness to resolve internal temperature gradients and the characteristic propagation time of volumetric Joule heat; and (4) both heat-load-pulse and current-pulse cases are validated against three-dimensional simulations and experiments, with the prediction error and computational speedup quantified.

2. System configuration and transient equivalent model

2.1. System configuration and modeling assumptions

The system under investigation consists of a single-hotspot chip, a thermoelectric cooler, and a microchannel heat sink. The total heat generation in the chip comprises localized hotspot power and uniformly distributed background power. Heat spreads within the chip and is then transferred to the cold side of the TEC. Under an applied current, the TEC pumps heat from the cold side to the hot side while simultaneously generating Joule heat. The total heat released at the hot side is conducted through the ceramic substrate, interfacial material, and solid structure of the microchannel heat sink to the channel walls, and is ultimately removed by the coolant.

To construct a reduced-order model suitable for rapid transient calculations, the following assumptions are adopted: the thermal and thermoelectric properties of the materials are constant over the temperature range considered; the Thomson effect and heat exchange between the external surfaces of the system and the ambient environment are neglected; the microchannel inlet temperature and flow rate remain constant during an individual transient event; and all components are represented using lumped thermal capacitances except for the thermoelectric legs, which are

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discretized along their thickness. The steady-state heat-transfer paths, spreading resistance, interfacial thermal resistance, and equivalent microchannel thermal resistance are calculated using the previously established steady-state figure [3].

2.2. Overall structure of the transient equivalent thermal-resistance network

In the steady-state model, the thermoelectric legs are represented by a single current-dependent thermal resistance. This treatment is adequate for determining the final equilibrium state but cannot explicitly represent the time-dependent effects of thermal energy storage, Peltier heat, and Joule heating within the thermoelectric legs. The transient model therefore retains the steady-state heat-transfer paths while explicitly introducing the thermal storage capacity and internal heat sources of the physical components. Under the thermal–electrical analogy, temperature corresponds to voltage, heat flow to current, thermal resistance to electrical resistance, and thermal capacitance to electrical capacitance. The energy balance at any temperature node i can be written as:

$$Ci\ dTi/dt\ =\ \Sigma j\ [(Tj\ -\ Ti)/Rij]\ +\ Qi(T,\ I) \tag{1}$$

where Ci is the thermal capacitance associated with node i, Rij is the thermal resistance between node i and adjacent node j, and Q̇i includes chip heat generation, Joule heating, and Peltier heat. Figure 1 shows the complete transient network. The hotspot temperature is connected to the chip-average temperature through a spreading resistance; the chip, ceramic substrate, electrodes, and microchannel heat sink are assigned corresponding thermal capacitances; the thermoelectric legs are represented by layered elements; and the coolant inlet temperature is imposed as a constant-temperature boundary [4].

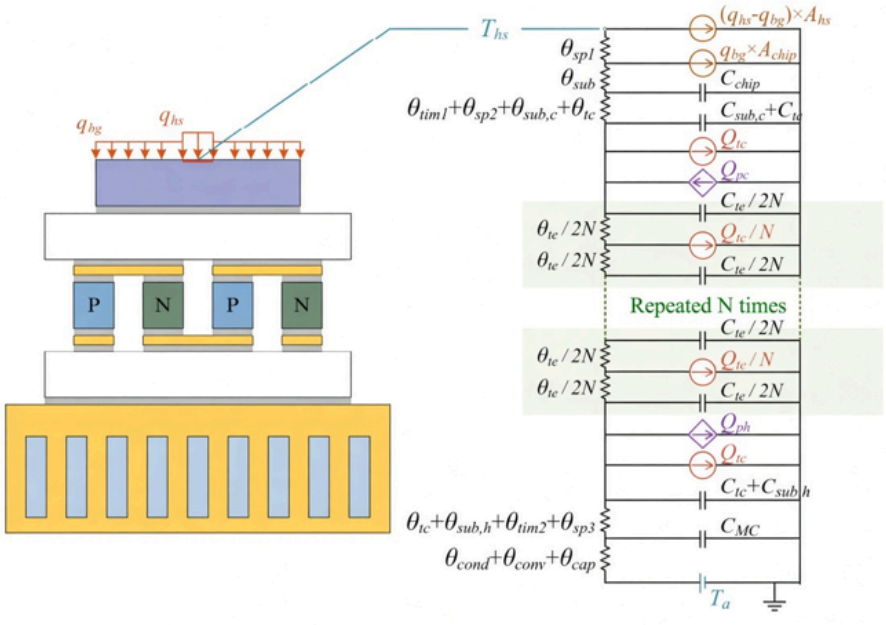


Figure 1. Transient equivalent thermal-resistance network of the thermoelectric–microchannel integrated hotspot cooling system

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2.3. Equivalent heat sources and thermal-capacitance parameters

The chip heat source is divided into the additional heat generation associated with the hotspot relative to the background region and the uniformly distributed background heat generation. These two sources are applied to the hotspot node and the chip-average-temperature node, respectively. Joule heating within the thermoelectric device consists of heat generated by the electrodes and contact resistance and volumetric Joule heating in the thermoelectric legs, expressed as:

$$Qtc = I^2 Rtc, \quad Qte = I^2 Rte \tag{2}$$

Peltier heat is generated at the cold- and hot-side interfaces between the thermoelectric legs and the electrodes, and its magnitude depends on both the input current and the interface temperature:

$$Qpc = Ste\ I\ Tc, \quad Qph = Ste\ I\ Th \tag{3}$$

where Ste is the effective Seebeck coefficient of all thermoelectric leg pairs, and Tc and Th are the cold-side and hot-side temperatures of the thermoelectric legs, respectively. Because the Peltier heat varies in real time with the node temperature, it is implemented as a temperature-controlled heat source in the model. The thermal capacitance of each component is calculated from its density, specific heat capacity, and volume as:

$$Ck = \rho k\ cp, k\ Vk \tag{4}$$

Where the thermal capacitance of the microchannel heat sink is taken as the sum of the capacitance of the solid region and that of the coolant participating in heat transfer. The thermal capacitance of the interfacial material between the chip and TEC has a significant influence on the early transient [5].

2.4. Distributed-parameter discretization of the thermoelectric legs

To capture the internal temperature gradient in the thermoelectric legs and the time delay associated with the propagation of volumetric Joule heat toward the cold and hot sides, all thermoelectric legs are discretized into N layers along the thickness direction. Each layer contains an individual conductive thermal resistance R_te/N, thermal capacitance C_te/N, and uniformly distributed Joule heat Q̇_te/N; Peltier heat is applied only at the cold- and hot-side boundaries. This discretization approximates one-dimensional transient heat transfer within the thermoelectric legs while maintaining a low number of degrees of freedom. Based on a layer-number independence study, N = 20 is adopted in this work [6]. Under the operating conditions considered, this discretization provides an appropriate balance between transient temperature accuracy and computational efficiency.

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2.5. Numerical implementation in MATLAB/Simulink

The transient network shown in Figure 2 is implemented in MATLAB/Simulink. Thermal resistances and thermal capacitances are represented by resistor and capacitor blocks, respectively. Chip heat generation and Joule heating are implemented as independent current sources, whereas Peltier heat is represented by a current source controlled by the relevant node temperature. The coolant inlet temperature is represented by a voltage source. The network connectivity automatically generates a system of ordinary differential equations, which are integrated using a fixed-step fourth-order Runge–Kutta solver [7].

The model inputs can accept arbitrary waveforms of TEC current and chip heat load, while the outputs record the hotspot temperature and the temperatures of the internal nodes. The model can therefore be used both for open-loop transient performance analysis and as a prediction model for subsequent controller design.

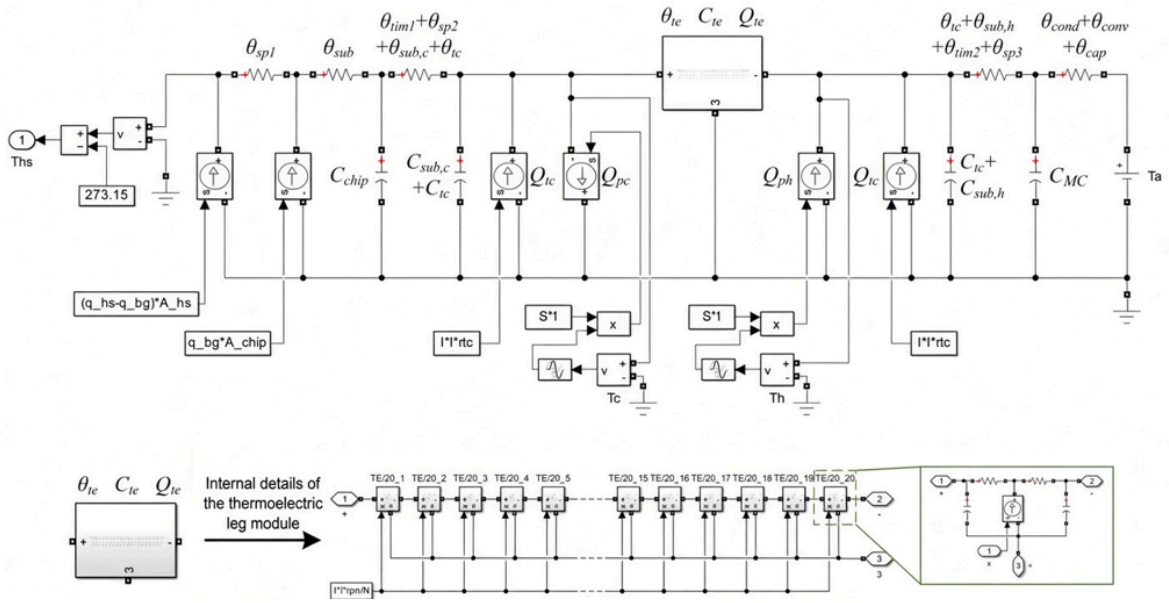


Figure 2. Transient network and layered implementation of the thermoelectric legs in MATLAB/Simulink

3. Model validation and performance assessment

3.1. Three-dimensional numerical model and experimental platform

A three-dimensional benchmark model is established in COMSOL Multiphysics and includes electric-current, solid and fluid heat-transfer, and laminar-flow fields. Thermoelectric effects and electromagnetic–thermal coupling are enabled in the thermoelectric-leg and electrode regions, while nonisothermal flow coupling is enabled in the microchannel region. A square hotspot is defined at the center of the chip, and the microchannel heat sink consists of a copper substrate with water cooling. The final mesh contains approximately 4.14 million elements, and the transient simulations are initialized from the corresponding steady-state solution.

The experimental (show in Figure 3.) sample consists of a 1.5 mm × 1.5 mm × 0.4 mm silicon-based thermal test chip, a commercial thermoelectric device (20035/024/015A), and a copper microchannel heat sink (LDHS1500). A 1 mm × 1 mm resistive array on the top surface of the chip

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serves as the hotspot heat source. Deionized water is used as the coolant, and the inlet temperature and flow rate are controlled by a constant-temperature bath and a peristaltic pump, respectively. The average hotspot temperature is measured using an infrared thermal imaging camera. Hotspot power, input current, flow rate, inlet temperature, and hotspot temperature are synchronously recorded at 0.5 s intervals. The equivalent thermal capacitance of the thermal interface material is fitted from the transient experimental data as 0.0047 J/K [8].

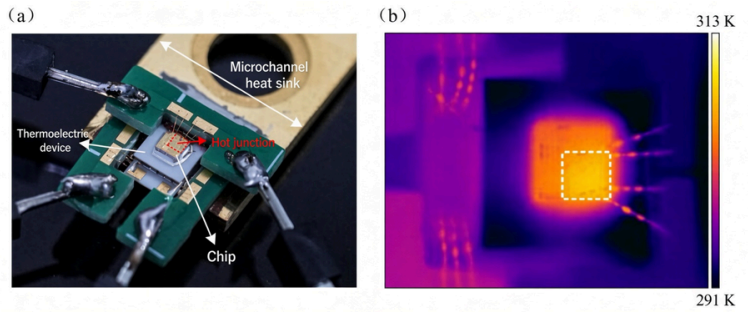


Figure 3. (a) Experimental sample; (b) infrared thermography measurement region

3.2. Convergence of layer number and time step

To eliminate the influence of the thermoelectric-leg layer number and time step on the results, the operating condition with the largest current pulse or the fastest temperature variation is selected as the reference case. The number of thermoelectric-leg layers N and the fixed time step Δt are varied independently. Using the high-resolution solution as the reference, the minimum hotspot temperature, maximum temperature deviation, time at which the extrema occur, and computational time are compared. The discretization parameters are selected when the changes in these metrics fall below the prescribed thresholds for $N \geq 20$ and further reductions in the time step.

3.3. Figures and tables

Two types of operating conditions are considered: square-wave pulses in chip heat load and square-wave pulses in TEC current. For each type, pulse durations of 3 s and 10 s are investigated. Heat-load pulses are used to assess the model response to external thermal disturbances, whereas current pulses are used to assess its representation of the coupled Peltier effect, Joule heating, and transient heat transfer within the thermoelectric legs [9].

Under the heat-load pulse conditions (Figure 4), the model accurately reproduces the heating, quasi-steady plateau, and cooling stages of the hotspot temperature response. The maximum relative errors for the 3 s and 10 s pulses are 0.99% and 0.75%, respectively. Under the current-pulse conditions, the hotspot temperature exhibits a heat-transfer delay relative to the current variation because heat propagates from the thermoelectric device to the chip. The predicted curves closely overlap the three-dimensional simulation results, with maximum relative errors of 0.77% and 0.78% for the 3 s and 10 s pulses, respectively.

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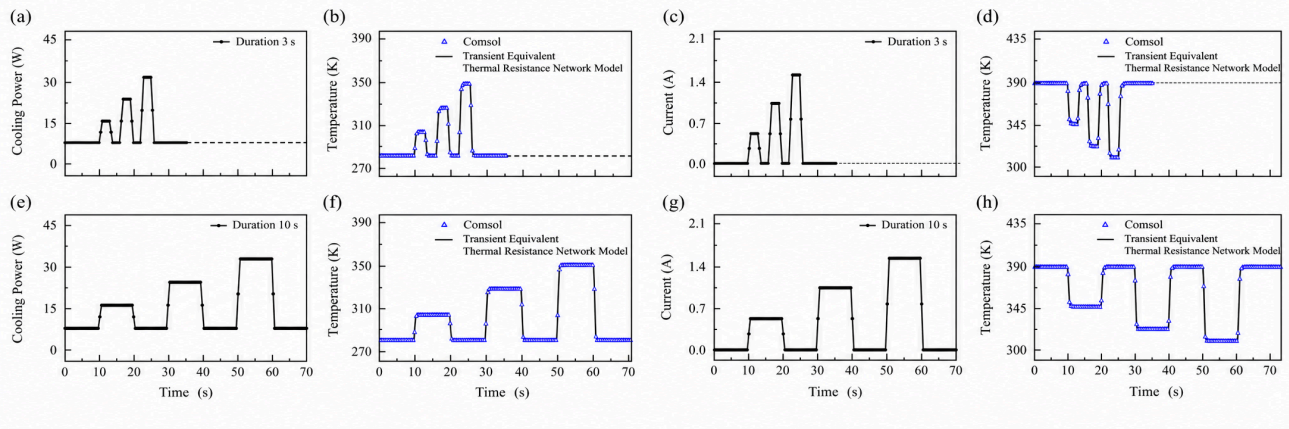


Figure 4. (a) Cooling Power Input — 3 s Duration; (b) Temperature Response — 3 s Duration; (c) Current Input — 3 s Duration; (d) Temperature Response — 3 s Duration; (e) Cooling Power Input — 10 s Duration; (f) Temperature Response — 10 s Duration; (g) Current Input — 10 s Duration; (h) Temperature Response — 10 s Duration

3.4. Experimental validation

In the experimental validation, 3 s and 10 s heat-load pulses and current pulses are applied in the same manner (show in Figure 5). The predicted and measured temperature histories show overall agreement during the heating, cooling, and recovery stages. For heat-load pulses of 3 s and 10 s, the maximum relative errors are 1.47% and 1.46%, respectively; for current pulses of 3 s and 10 s, the maximum relative errors are 1.61% and 1.48%, respectively [10].

The largest discrepancies occur near the beginning and end of the pulses. On the one hand, the actual thermal capacitances of the individual components and the interfacial thermal capacitance of the experimental sample are difficult to determine precisely. On the other hand, the 0.5 s sampling interval cannot fully resolve the rapid temperature changes. Once the system enters a quasi-steady regime, the error level of the transient model becomes comparable to that of the steady-state model [11].

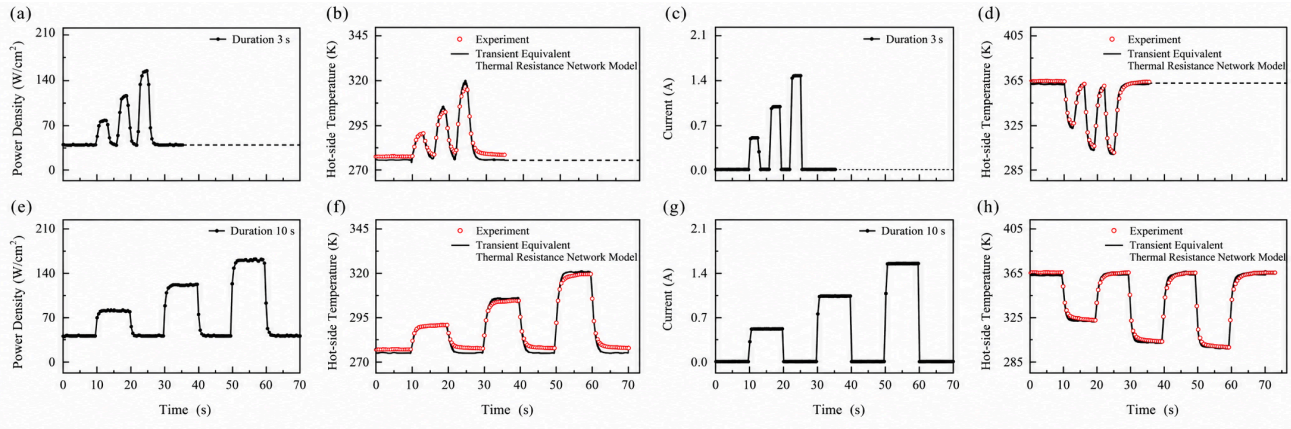


Figure 5. (a) Power Density Input — 3 s Duration; (b) Hot-side Temperature Response — 3 s Duration; (c) Current Input — 3 s Duration; (d) Hot-side Temperature Response — 3 s Duration; (e) Power Density Input — 10 s Duration; (f) Hot-side Temperature Response — 10 s Duration; (g) Current Input — 10 s Duration; (h) Hot-side Temperature Response — 10 s Duration

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3.5. Computational efficiency and applicability

For the operating points included in the heat-load-pulse validation, the transient equivalent thermal-resistance network model requires approximately 4 s to complete the calculations, whereas the corresponding three-dimensional COMSOL transient simulations require approximately 20 h. The computational speedup therefore exceeds three orders of magnitude, enabling rapid operating-condition sweeps, structural parameter studies, and controller iteration [12].

3.6. Demonstration of transient subcooling

To demonstrate the ability of the model to capture the different characteristic time scales of thermoelectric systems, a short-duration current-pulse case is retained. When a current step is applied, the interfacial Peltier effect increases immediately, whereas the propagation of volumetric Joule heat toward the cold side requires a finite time (show in Figure 6). Consequently, the hotspot temperature first decreases rapidly and then rises as Joule heat accumulates. This result demonstrates that the model not only reproduces the input–output response but also captures the underlying physical mechanism of transient subcooling.

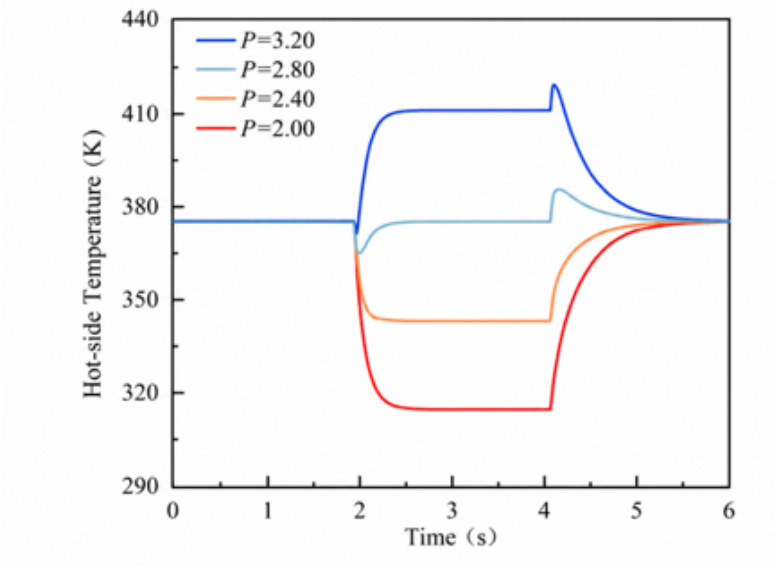


Figure 6. Transient subcooling responses at different current-pulse amplitudes

4. Conclusions

A system-level transient equivalent thermal-resistance network has been developed for rapid prediction of thermoelectric–microchannel integrated hotspot cooling systems. The model provides a unified representation of hotspot spreading in the chip, the Peltier effect and Joule heating within the thermoelectric device, thermal energy storage in the system components, and heat rejection through the microchannel heat sink. A 20-layer distributed-parameter representation of the thermoelectric legs captures their internal transient temperature response. For 3 s and 10 s heat-load and current pulses, the maximum relative error is below 0.99% relative to the three-dimensional simulations and below 1.61% relative to the experimental measurements. For 71 transient operating points, the proposed model requires approximately 4 s, compared with approximately 20 h for the corresponding three-dimensional simulations, resulting in a computational speedup of more than

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three orders of magnitude. The model is therefore suitable for rapid transient-condition sweeps and control-oriented design.

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