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Moore's Law: Fundamental and Technological Challenges

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Abstract. This paper discusses the fundamental and technological challenges for continuing the shrinking of transistor size under Moore's Law. Over the past few decades, making transistors smaller has boosted chip performance, reduced the cost per transistor, and supported the development of integrated circuits. However, as transistors become smaller and smaller, the traditional method of scaling is facing increasingly significant limitations. On the physical side, quantum tunneling, short-channel effects, material limits, and heat dissipation all impair the stability and reliability of transistors. On the technological side, lithography limits, manufacturing errors, yield problems, and the complexity of 3D integration have made further chip development more difficult and costly. Facing these challenges, the future of semiconductor technology should not solely depend on simply reducing transistor size. Instead, it requires the combined development of Tao's Law, alternative materials, and 3D integration. In conclusion, faced with obstacles including physical objective limitations and technical limitations, the future of Moore's Law is more likely to depend on progress in materials, structures, and manufacturing technologies, rather than only on traditional size scaling.

Keywords: Moore's Law, transistor scaling, integrated circuit

1. Introduction

Moore's Law states that the number of transistors on an integrated circuit doubles approximately every 18 to 24 months, leading to a corresponding increase in computing power and a decrease in relative cost [1]. As transistor scaling, it increases GPU and CPU performance, reduces manufacture input, and new functions. The history of transistor scaling can be roughly generalized to eight periods. The eight periods are respectively the Vacuum Tube Era, First-Generation Transistor Era, Silicon Transistor Era, Integrated Circuit Era, MOSFET and CMOS Era, Very Large-Scale Integration Era, Three-Dimensional Transistor Era, and Post-FinFET Era. Released in June 2026, WSTS data shows AI development fuels semiconductor expansion. Logic and memory chips are

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growing by 37% and 250%, respectively [2]. However, physical limitations restrict its further improvement, marking the gradual failure of Moore's Law [3].

Until now, the transistor has become extremely difficult. The challenge can be divided into three parts: First, physical limits including short-channel effect, random dopant fluctuation, and collapse of Dennard Scaling [4]. Second, the limitations of materials and device structures, such as Soaring Source-Drain Contact Resistance, Mobility Saturation of Silicon, and New Challenges of GAA & CFET [5]. Third, economic cost, which is caused by exponentially increasing research and development costs [6]. Those issues need to be resolve. There are five main reasons for limiting the continuing scaling of the transistors: the short channel effects, quantum tunneling effects, fundamental limitations, heat dissipation problems and inadequate two-dimensional materials [7]. The quantum tunneling effect is a quantum-mechanical phenomenon. Particles pass through an energy barrier it is not supposed to be able to cross under classical physics environment, this phenomenon is called the quantum tunneling effect [8].

Short channel effects are a series of effects that weaken the gate's control over the channel when the channel length of a MOSFET becomes too small [4]. The fundamental material limitations are physical limitations caused by intrinsic properties of materials, which are caused by the material itself [7]. Heat dissipation occurs when the transistors are so dense that the heat generated by the transistors cannot be removed efficiently [9]. Inadequate two-dimensional materials are limited by difficult manufacturing, defects, high contact resistance, and poor stability [10]. The five limitations above are the major barriers we need to overcome in the future to continue shrinking the size of the transistors [7].

Technologically, we discuss these two key reasons: lithography limits and Manufacturing variability and yield issues [11]. Lithography is the core technology that determines transistor dimensions; it uses short wavelength waves to transfer circuit patterns onto silicon wafers [12]. However, as transistors scale smaller, traditional lithography can no longer achieve the required precision and accuracy [12]. From the perspective of variability and yield, as transistor dimensions become smaller, even minute defects can result in the total failure of an integrated circuit, but we can not avoid errors occurring [13]. These technological facts prevent manufacturers shrink transistors size further [11].

In this review, we conclude on currently developed coping strategies and prospective solutions, including 3D integration, the application of Tao's Law, and the replacement of silicon with other materials [14]. Based on previous studies and the authors' own synthesis and reflection, this paper summarizes the challenges faced by traditional chips and corresponding feasible solutions, providing a reference for future research and development.

2. Physical limitations

2.1. Quantum tunneling effect

Among all the obstacles holding back transistor scaling, quantum tunneling became the first unavoidable industrial block. Around 2005, Moore's Law demanded continuous thinning of the silicon dioxide gate dielectric layer in order to strengthen the gate control over the channel. When the process scaled down to a certain size, the oxide layer became small enough to cause the quantum tunneling effect. According to the experiment done by Pearl Bipin Pulickal, it clearly identifies that there are four phases related to transistor scaling, in which phase 1 to phase 2 is directly related to the quantum tunneling effect. In Phase 1, transistor sizes shrink initially; the technology benefits from increased performance and reduced power consumption. However, as approaching the

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nanometer scale, significant quantum mechanical effects can be observed. At Phase 2, at dimensions close to 10-10 meters, electrons within the transistors are no longer governed solely by classical mechanics. Instead, their behavior is dominated by quantum mechanics. Two primary phenomena come into play [15]. This shift between the two phases reveals Moore's Law's physical bottleneck. Phase 1 gains benefits from classical scaling, while Phase 2 brings quantum tunneling.

This phenomenon led to severe consequences for integrated circuits. First, as elements of silicon transistors have shrunk to the scale of atoms and molecules, quantum tunnelling and leakage currents make it increasingly difficult to keep them reliably switched off, limiting further scaling [16]. Second, continuous leakage current produces massive heat and energy loss, leading to significant power dissipation and deteriorated thermal stability. Third, these long term abnormal current leakage and continuously high heat will speed up the aging of the chip, making them more easily to break down.

2.2. Short-channel effects

The short channel is a major reason that obstacle we to shirk the size of transistors. In a MOSFET system, the gate voltage controls the potential between source and drain, which allows the transistor to switch between on and off states. However, until the channel length reaches a nanometer scale, the electric fields of the source and drain start to influence the efficacy of the gate. The gate will lose the ability to control the electrostatic potential, leading to the failure of the transistor.

The main reason for the short-channel effect is that the drain electric field of the drain might penetrate the source. When the high drain voltage lowers the source- channel energy barrier, the drain-induced barrier lowering effect occurs. The electrons can enter the channel easily, so the threshold voltage decreases as the drain voltage increases. At the same time, the threshold voltage will decrease as the channel becomes shorter because of charge sharing between the gate and source-drain depletion regions. The depletion regions may start to punch through if the distance between channels continues to decrease while there is no improvement in gate control, especially in the insulation capacity. If the gate loses control of the transistor, there will still be electrons in the transistor while the transistor should be in an off state. These effects show that when the channel length continues to decrease, the channel potential will be controlled more by the drain instead of being fully controlled by the gate, which reveals a limitation of Moore's Law: shorter channels increase switching speed but weaken the gate's control and reliability. Although a shorter channel can reduce the scattering proportion during carrier transport, interface roughness and interface defects at the oxide-semiconductor boundary are still important scattering sources. These defects can reduce the carrier's mobility and reliability of the transistors [1].

Short channel effects will lead to several serious consequences for the chip. First, the total amount of off-state leakage current will be a huge number; even though a single transistor doesn't waste much, the total amount will be amplified by billions of transistors. The transistors will waste power and generate heat even when they are not switching, which decreases the performance of the chip and increases the energy requirement. In addition, the reduced threshold voltage and degraded subthreshold behavior make the difference between the on and off state unclear, increasing the logic errors of the chips, which make the chips less reliable. Third, the strong electric field near the drain can accelerate the charge carriers and lead to hot-carrier degradation, which reduces the long-term reliability [17].

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2.3. Fundamental material limits

Silicon is the dominant semiconductor material because of its moderate band gap, the native silicon dioxide interface, and the compatibility with large-scale manufacturing. Back to the period when silicon became popular in this field, researchers realized that the band gap of silicon is very suitable for making MOSFETs, which is 1.12 eV at room temperature (300 K). Furthermore, the SiO_2 grown by thermal oxidation of silicon forms an interface that gives an ultra-low defect density that enables high carrier mobility. Therefore, people chose silicon rather than Ge and developed large-scale semiconductor manufacturing.

However, when the size of MOSFETs continues to shrink in accordance with Moore's Law, the scaling of silicon-based CMOS is approaching its material limits. First, for maintaining electrostatic control, it is necessary to reduce the equivalent oxide thickness (EOT) of gate dielectrics [5]. When the thickness of SiO_2 layers is reduced to a few atomic layers, electrons will tunnel through the gate oxide and cause an increase in gate leakage current [1]. Therefore, it is challenging to make SiO_2 layers thinner due to the significant increase in gate leakage current [6]. The rise in gate leakage current may be the main reason leading to the limited extendibility of SiO_2 [6]. Moreover, inversion layer quantization and the polysilicon-gate depletion effect will lead to the loss of inversion charge and transconductance in the thin gate oxide [1].

Si/SiO_2 interfaces have surface roughness, which is inherent to them and can lead to surface scattering [4]. Surface scattering becomes significant when the size of electronic devices decreases to nanoscale thicknesses [4]. This is because charge carriers are confined closer to the Si/SiO_2 interface, where surface roughness, interface defects, and impurities have a greater influence on carrier transport [4]. It enhances the interaction between charge carriers and those in the thin channels, which in turn significantly degrades carrier mobility [7]. As a result, these scattering mechanisms interrupt carrier transport and reduce the effective carrier mobility [4].

In conclusion, although silicon has been the dominant semiconductor material for CMOS technology due to its suitable properties, continued device scaling has revealed several fundamental material limits. These challenges have motivated the exploration of alternative materials, which are discussed in the following section.

2.4. Heat dissipation

In the early era of Moore's Law, transistor miniaturization was governed by Dennard scaling. Dennard scaling theory holds that shrinking transistor dimensions can be balanced with heat dissipation. As transistor dimensions and supply voltage shrink proportionally, this combined effect ensures that power density remains approximately constant [18, 19]. Thus, heat generation does not increase with higher integration density, and thermal overload does not occur. However, when transistors are scaled below 65 nm, Dennard scaling effectively collapses and transistors enter the leakage-limited regime [19, 20]. As shown in the data in Table 1, with further miniaturization and constant total area, when the number of transistors rises by a factor of S^2, it requires a lower threshold voltage V_{th}, and$_{the}$ supply voltage V_{dd}^2 needs to decrease to $1/S^2$ in the Dennardian era. In contrast, decreasing V_{th} leads to quantum tunneling effects and triggers exponential leakage current in the post-Dennardian era. To restrain static power consumption, designers cannot continuously reduce $V_{th,}$ and therefore V_{dd}^2 is approximately constant too. The overall result is that power density surges sharply as transistor dimensions shrink, and transistor utilization declines to $1/S^2$.

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Table 1. Transistor property in Dennardian era compared with that in post-Dennardian [18, 21]

Transistor Property	Dennardian	Post-Dennardian
ΔQuantity	S^2	S^2
ΔFrequency	S	S
ΔCapacitance	1/S	1/S
ΔV^2_{dd}	$1/S^2$	1
⇒ $\Delta Power= \Delta QFCV^2$	1	S^2
⇒ ΔUtilization= 1/Power	1	$1/S^2$

Even with advanced packaging techniques, the fundamental thermodynamic theories restrict the maximum thermal affordability on silicon chips. There are three basic thermodynamic limits. The Landauer principle states that no bit of information can be erased without energy generation. $E_{bit}=k_BTln2$, proving that waste heat generation during computing with erasing is unavoidable [22]. Besides, Newton's law of cooling $Q=hA\Delta T$, gives a fixed maximum for heat dissipation, which depends on packaging, thermal interface materials, and other hardware. In addition, Carnot's theorem shows that cooling devices also consume extra power and cannot dissipate all the heat produced by both transistors and cooling devices [22].

3. Technological limitations

3.1. The unprecedented challenges of lithography

At the present stage, the employment of Lithography has emerged as a restricting factor for the advancement of transistor devices.

The initial segment of the operational limitation corresponds to the practical implementation workflow. As transitional substitute options for EUV technology, the implementation of DUV multi-patterning (SADP/SAQP) gives rise to the accumulation of overlay deviations, elevated incidence rates of wafer failure and the rise of manufacturing expenses by 30%–50% [12], rendering it incapable of lending support to the steady operation of mass production for process nodes of 3 nm and finer specifications [11]. High-NA extreme ultraviolet lithography also encounters inherent process-related constraints [13]. The raised magnitude of its numerical aperture brings about mask shadowing impacts and obligatory re-engineering of the photomask [13]. The reduced exposure field dimension necessitates higher-velocity scanning, lifting the bar for mechanical and thermal control benchmarks and further driving up the cost of manufacturing operations [13].

The second segment of restriction relates to expenditure and production capability. Cutting-edge lithography apparatuses incur exorbitant expenses. EUV and High-NA EUV scanners are priced at $150–200 million and $400 million per unit respectively [23], a situation that has secured exclusive control of advanced fabrication capacity within foremost semiconductor foundries and has erected obstacles for small and medium-sized enterprises to access the tape-out procedures of advanced process nodes [14]. The sophisticated fabrication supply networks of extreme ultraviolet lithography have brought about diminished production yield and a delivery cycle of more than 18 months [14], which fails to satisfy the rising requirement for cutting-edge artificial intelligence chips. Centralized provision of auxiliary components also renders the manufacturing operation of semiconductor fabs

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vulnerable to fluctuations in the entire supply network [11]. The supporting resources and experimental infrastructure of the research team further elevate the expenses of chip manufacturing procedures [14]. The downward cost trajectory characteristic of Moore's Law has come to a complete halt [3], which has imposed obstacles on the widespread adoption of advanced semiconductor products.

The third segment of restrictive factors covers geopolitical dynamics and supply chain systems. The exclusive market dominance of ASML in the domain of cutting-edge lithography apparatus, together with the global dependence on component procurement, has brought about notable fragility of the supply network and cross-border regulatory limitations from geopolitical dimensions [11], which has imposed constraints on the regional capability of high-end manufacturing and amplified the global technological disparities of the semiconductor industry [11]. Key supporting supplies and testing apparatus have also been subject to worldwide monopolization [24]. Prolonged industrial validation has rendered the achievement of full-chain technological advancements in cutting-edge lithography exceptionally challenging [24].

3.2. Manufacturing variability and yield

Another major obstacle to continuously decreasing the size of transistors is the variability during the manufacturing process. As the dimensions of a transistor. Since the size of the transistors approach to nanometer scale, the fault tolerance will be low so that even a small manufacturing error can become subversive error to the chip. it is impossible for any manufacturer to produce billions of transistors with the same dimensions and material properties. Small variations in channel length, doping concentrations, oxide thickness and the edges formed during the lithography process will all lead to the invalidation of the transistor, which has been designed to be identical in its properties [25].

There are numerous reasons leading to the variation of the transistors. Random doping fluctuations are one reason that leads to variability. Dopant atoms will be added into the semiconductor materials, determining the electrical properties. However, the amount and position of individual dopant atoms become important since the transistors become tiny. Variations in the number or location of those atoms will lead to a significant change in threshold voltage and the current in the transistor. Variations in channel length can also affect the electric field and the switching ability of the transistor. Line-edge roughness is another major variability. The imperfect smoothness of the production process at the nanometer scale will lead to line-edge roughness, which will change the actual channel length or width. The gate control and leakage current will also be affected by the variation in the thickness of the oxide layer. As transistor dimensions continue decreasing, the small variations will become significant and make up a large percentage of the total device size, which will make process variability increasingly precarious [25].

Manufacturing variability is also affected by the yield of semiconductor production. The percentage of manufactured devices that operate correctly within the required specifications is yield. During the material synthesis, patterning, deposition, and other fabrication processes, defects and variations will be introduced, which might lead to different characteristics such as threshold voltage, carrier mobility, and leakage current. However, when those small defects convene, it might lead to a complete failure of the chip's performance. In that case, increasing the density of transistors while maintaining a high manufacturing yield becomes challenging [26].

Manufacturing variations is another limitation for Moore's law. Even if it is possible in theory to produce smaller transistors, the process must also ensure the yield with a huge number of transistors. Both the yield and reliability of the chip will be reduced while the variability increases, which will

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also require additional process control and testing, leading to increased manufacturing complexity and cost. Therefore, future transistor scaling will not solely depend on smaller structures but also on controlling materials and manufacturing processes [25, 26].

4. Current solutions and future directions

4.1. Tau Scaling Law

As Moore's Law slows, there are several challenges that prevent geometrical shrinking. So, the Tau Scaling Law provides an alternative way to improve computing performance. Its core logic is time scaling.

The core of this law is to reduce the end-to-end characteristic time constant (τ) to get better performance. $\tau = f(\tau transistor, \tau circuit, \tau chip, \tau system)$, meaning τ values of four layers: device switching delay, circuit-level RC delay, chip-level memory access latency, and system-level communication latency [27]. Thus τ scaling expands the optimization variable from shrinking dimension to parasitic resistance, capacitance, interconnect topology and system protocols [28].

Improving τ scaling requires two mutually reinforcing directions: Chiplet technology and 3D packaging. Chiplet splits a monolithic SoC into multiple functional chiplets and reintegrates them together by advanced packaging. This technology can effectively reduce τ_{chip} and τ_{system} even with a little increase in Die-to-Die delay [29]. Dividing large dies into smaller chiplets can improve yield; for example, a 360mm^2 monolithic die has a yield of about 15%, while a four-chiplet design can increase yield to 37% [30]. Also, chiplets with different functions can be manufactured by their respective optimal process to get an overall better performance [30]. After chiplet division, 3D packaging is needed to integrate them in the vertical direction to compress τ_{system} and τ_{chip}. LogicFolding folds critical path logic from a plane into vertically stacked active tiers and keeping interconnection by ultra-fine-pitch hybrid bonding. By developing these technologies, chiplet provide a way to get flexibility of modular partitioning and 3D packaging provides high-density vertical interconnection. These technologies work together to get a complete and effective loop of τ scaling from device to system to get better performance [27, 30]. As in the Kirin 2026 test chip, these technologies, especially 3D packaging and chiplets, in a lab environment provide a 55% step-wise increase in transistor density and a 41% reduction in power consumption at a fixed device node. In addition, its CPU performance-core frequency increases from 2.75GHz to 3.1GHz [27].

4.2. Alternative materials

Since silicon-based CMOS technology is approaching its fundamental scaling limits, alternative channel materials have been investigated for future transistor technologies. First are two-dimensional materials (2DMs), such as MoS_2, WS_2, WSe_2, $MoTe_2$, and InSe. These kinds of materials became popular due to their atomically thin structures and electrical properties [31]. Compared to conventional silicon channels, 2DMs can maintain atomic-scale thickness while preserving their electronic properties. Their atomically thin structure provides stronger electrostatic control by the gate electrode, which helps suppress short-channel effects when transistor dimensions continue to shrink [31]. Also, the surfaces of 2DMs are inert with negligible dangling bonds. As a result, they form cleaner interfaces with lower defect densities when forming heterostructures [31]. Reducing interface defects can reduce carrier scattering and improve carrier transport performance compared with extremely scaled silicon channels [31]. Studies have demonstrated that when transistor channels are scaled below 1 nm, 2D semiconductors can maintain higher carrier mobility

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than silicon because of reduced surface scattering and improved electrostatic control [31]. However, 2DM-based transistors still face several challenges before practical applications. Large contact resistance between metal electrodes and 2D materials limits the driving current, which remains inferior to conventional silicon devices [7].

To overcome the scaling limitation of conventional SiO_2 gate dielectrics, using high-κ materials is an alternative solution [5]. High-κ dielectric materials, especially HfO_2, have been used as gate dielectric materials due to their high dielectric constants and compatibility with CMOS technology [5]. Compared to SiO_2, high-κ materials have higher dielectric constants. They not only allow physically thicker dielectric layers, but also maintain a small EOT. This property reduces the probability of electron tunneling through the dielectric layer and decreases the gate leakage current [5]. Also, using high-κ materials as gate dielectrics can reduce EOT and operating voltage [32]. HfO_2 is one of the typical high-κ materials because it contains an appropriate dielectric constant (around 20). Extremely high dielectric constants are associated with reduced band gaps, which will increase direct tunneling leakage and limit further scaling [5]. However, replacing SiO_2 with high-κ materials faces new challenges, including interface defects, charge trapping, and mobility degradation, which are caused by poorer dielectric/channel interfaces.

5. Conclusion

This paper systematically reviews the historical progression of transistor scaling and delves into the key bottlenecks currently constraining the development of Moore's Law [33]. The study shows that the traditional approach of relying solely on shrinking transistor feature sizes to improve performance has reached its limits in both physics and technology [34].

At the physical level, as feature sizes enter the nanoscale, quantum tunneling [15] and short-channel effects [35] limit device switching performance severely, while material limitations with heat dissipation and cooling challenges limit further scaling [36]. Even two-dimensional materials, considered promising alternatives, still face scaling shortcomings [37]. At the technological level, the limits of lithography technology [38], variations in manufacturing processes, and yield losses [39] further restrict the scaling of transistors.

Faced with these obstacles, the future evolution of the semiconductor industry needs to shift from "scaling down in size" to "scaling down in functionality." As Tao's Law suggests, performance improvements should not rely solely on process advancements, but should actively search for alternative materials [40](such as those surpassing the physical limits of traditional SiO2), 3D integration [41], and other architectures. The Tau scaling law proposed by Huawei shares similar ideas [42], while focusing on the synergistic effects among these three elements—materials, processes, and architecture. In summary, chip development in the post-Moore era will require much more innovation from physics, materials science, and microelectronics engineering. The synergy of these fields will likely serve as the ultimate path for transistor scaling.

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